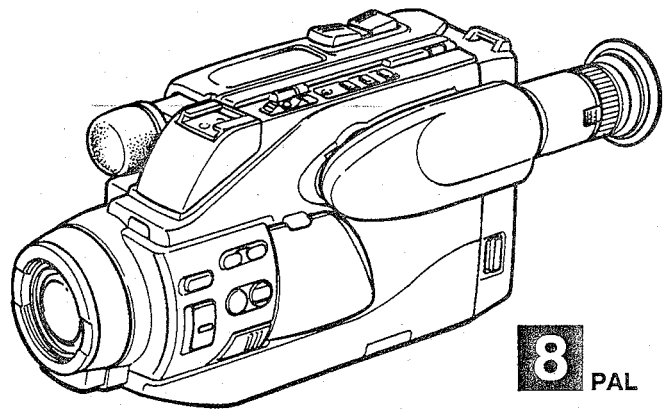
SANYO

TRAINING MANUAL

8 mm Camcorder

VM-RZ1P
(GERMANY, SWITZERLAND, ITALY, U.K., SPAIN, MIDDLE EAST, AUSTRALIA,)

VM-D9P
(U.K.)



Specifications

Television system	PAL, CCIR
Video recording system	Rotating 2-head helical-scan system
Audio recording system	Rotating head FM system
Cassette type	8 mm video cassette tape
Tape speed	SP : 20.051 mm/sec. LP : 10.025 mm/sec.
Recording/playback time	90 minutes (P5-90 cassette) SP mode 180 minutes (P5-90 cassette) LP mode
Fast forward/rewind time	Approx. 7 minutes (P5-90 cassette)
Pickup element	CCD solid-state type (320,000 pixels)
Viewfinder	Electric (0.6 inch type, black and white)
Lens	Electro powered 8×zoom lens f= 6 mm ~ 48 mm F1.8 Filter diameter : 37 mm
Focus	Full-range fuzzy logic auto-focus
White balance	Fuzzy logic auto white balance
Iris	Fuzzy logic auto iris
Minimum subject illumination	2 lux (Low light mode)
Subject illumination range	2 ~ 100,000 lux
Recommended subject illumination	300 lux or more (In normal mode, other modes such as Auto high speed shutter mode may need more light.)
Power supply voltage	DC input 6 V (battery pack) / 6.5 V (AC adaptor/charger)
Power consumption	5.6 W during camera recording
Operation temperature range	0 ℃ ~ 40 ℃ (32 °F ~ 104 °F)
Storage temperature range	− 20 ℃ ~ 60 ℃ (− 4 °F ~ 140 °F)
Dimensions (W) × (H) × (D)	116 × 118 × 259 mm
Weight	770 g (1.70 lb) approximate not including battery pack, cassette and grip belt
Microphone	Electret condenser type (omnidirectional)
Video terminal	Video output 1 Vp-p, 75 ohm unbalanced, negative sync
Audio terminal	Audio output − 7 dBs, 2.2 kohm or less
Earphone jack	Mini jack, for 8 ohm earphone

VM-RZ1P
PRODUCTION CODE No.
126 023 00 (GERMANY)
126 023 03 (SWITZERLAND)
126 023 05 (MIDDLE EAST)
126 023 06 (ITALY)
126 023 07 (U.K.)
126 023 08 (AUSTRALIA)
126 023 09 (SPAIN)

VM-D9P
PRODUCTION CODE No.
126 023 14 (U.K.)

* Specifications and external appearance are subject to change without notice.

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1. GENERAL

This is new model of a compact light-weight 8-mm camcorder.
The features are as follows :

1) Fuzzy Auto Focus (Fuzzy AF)
In addition to the characteristics accompanied by the digital auto focusing system, it has become possible, through the application of the fuzzy theory, to attain and determine finer information and contents of the picture, and have further accuracy on the auto tracking system.

2) Fuzzy Auto Iris (Fuzzy AE)
Through the application of the fuzzy theory, the auto iris which have become closer to the human eyes has been attained, it has become possible to lessen the blacklighting effects in counterlight, and take a much more beautiful picture.

3) Fuzzy Auto White Balance (Fuzzy AWB)
The color is compensated more accurately by applying the fuzzy theory and inferring the color condition of the subject from color phase, distribution, amount of high-frequency component, etc.

4) Auto Date
The Auto Date function is constantly powered by a lithium battery. Once the date is set, it is automatically incremented.

5) High Speed Shutter
Even when the fast moving subject is recorded, the slow or still picture does not get blurred. Shutter speed is set automatically between 1/250 and 1/10,000 sec. depending on the brightness. (Shutter with continuously variable speeds).

6) × 8 Power Zoom Lens
From a wide shot to a close-up, it provides an 8:1 zooming effect.

7) Electronic Viewfinder (Black and White)
The electronic viewfinder serves as a built-in black-and-white monitor during recording and playback and displays a wide variety of helpful data during recording.

8) Smooth Editing by Flying Erase Heads
The incorporation of flying erase heads allows smooth editing of new material in the middle of previous recording.

9) Linear Time Counter
The tape travel is displayed in hours, minutes and seconds, allowing you to check the remaining tape time easily.

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2. CAMERA CIRCUIT DESCRIPTION

2-1. CCD IMAGE DEVICE

2-1-1. Outline

This system employs a 1/3 inch optical size interline type CCD solid image device. The structure and characteristic of the device are shown below, and block diagram is shown in Fig. 2-2.

[Structure]

- Optical size 1/3 inch format
- Interline type CCD image sensor
- Effective picture elements 500(H) × 582(V)
- Picture elements in total 537(H) × 597(V)
- Chip size 6.3mm(H) × 5.4mm(V)
- Unit cell size 9.8 μm(H) × 6.3 μm(V)
- Optical black Horizontal(H) direction Front 7 picture elements, Back 30 picture elements, Vertical (V) direction Front 14 picture elements, Back 1 picture element
- Dummy bit number Horizontal : 16, Vertical : 1(only in even fields)

[Characteristic]

- Field accumulation system with high movement resolution
- Low darkness current, high sensitivity sensor
- Ye, Cy, Mg, G complementary color mosaic filter
- Horizontal register and pre-charge gate 5V direct drive system
- Low smear and low blooming
- Variable speed electronic shutter function

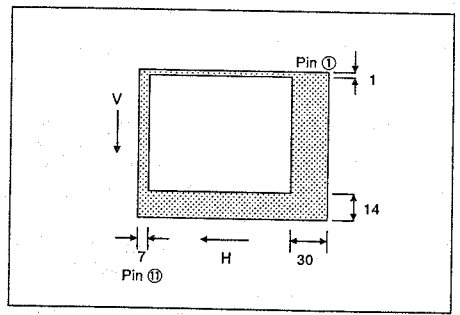


Fig. 2-1. Optical Black Location (Top view)

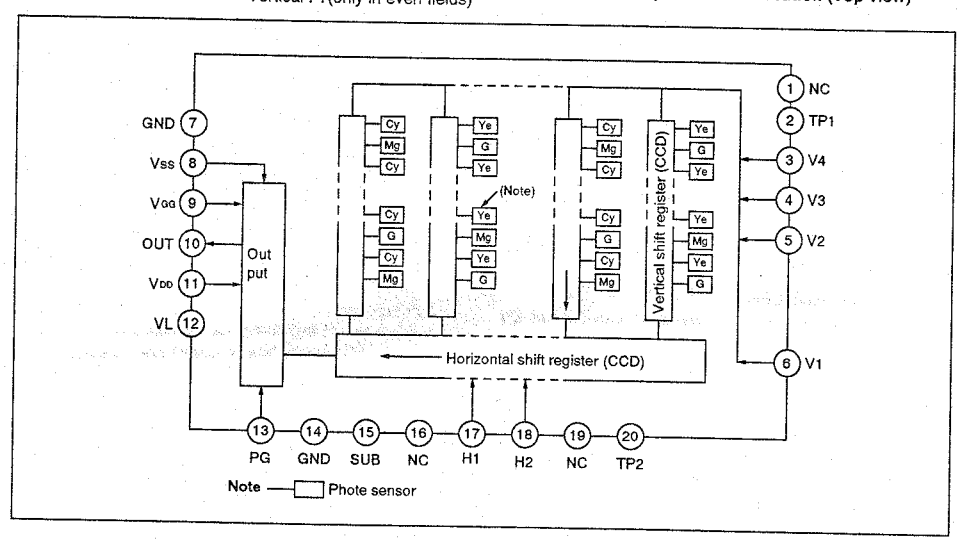


Fig. 2-2. CCD Block Diagram

2-1-2. V Register Operation

In this system, V register size is made compact because there are so many picture elements. So, for the transfer of V register, 4-phase drive system with a large dynamic range is employed.

Though the drive circuit becomes complex according to 4-phase drive system, handling electric charge per electrode is large.

The model chart of the 4-phase drive is shown in Fig. 2-3.

V register has 4 electrodes (V1 to V4).

In step ①, signal electric charge is in the well of electric charge of V1 and V2 because the electric potential is high in V1 and V2 and low in V3 and V4, In step ②, electric potential of V3 becomes high and the signal electric charge spreads through the well of electric charge of V1, V2 and V3 because the electric potential of V1 becomes low. Compared with step ①, there is a difference of 1 electrode (1 electrode transfer).

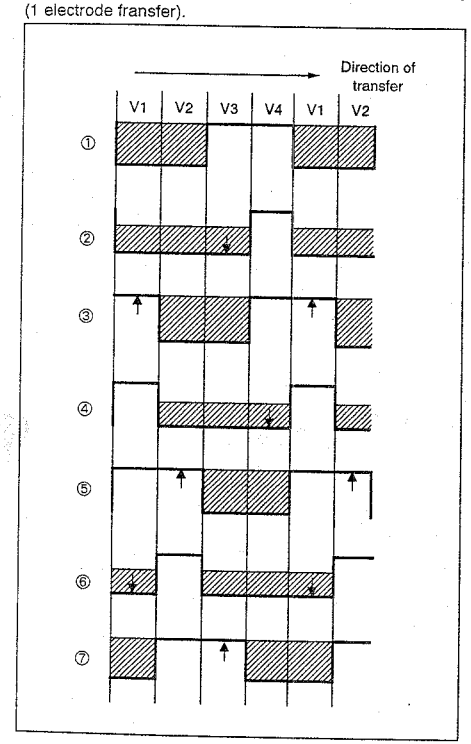


Fig. 2-3. 4-Phase Drive Model Chart

2-1-3. V Register Read Operation from Light Receiving Section

This system employs the 3-value drive V register as shown in Fig. 2-4.

During transfer V register, the applied voltage charge on the V register electrode is low. Therefore, the electric charge of the signal cannot get out from the light receiving section. However, since the electric charge during reading becomes high, the electric charge of the signal is transferred to the V register.

Further explanation is described in the following.

Transfer operation to the V register from the light receiving section in odd field is shown in Fig. 2-5. In Fig. 2-5, V1 to V4 change as shown in ① to ⑭. When each of V1 to V4 is −9V, the potential of the V register becomes a barrier and it becomes well when they are 0V. The potentials of V1 and V3 and that of the sensor gate become the lowest well in the conditions of ③ and ⑤. So, the signal electric charges from the sensor section of 2n+1(line) and 2n(line) move to V1 and V3, respectively. The signal electric charges generated at ⑦ between two adjacent picture elements are mixed within the V register, and transferred as shown in ⑧ to ⑭.

The case of the even field is shown in Fig. 2-6. The difference from the case of the odd field is that a combination of picture elements differs when mixing the signal electric charges between adjacent picture elements at ⑦.

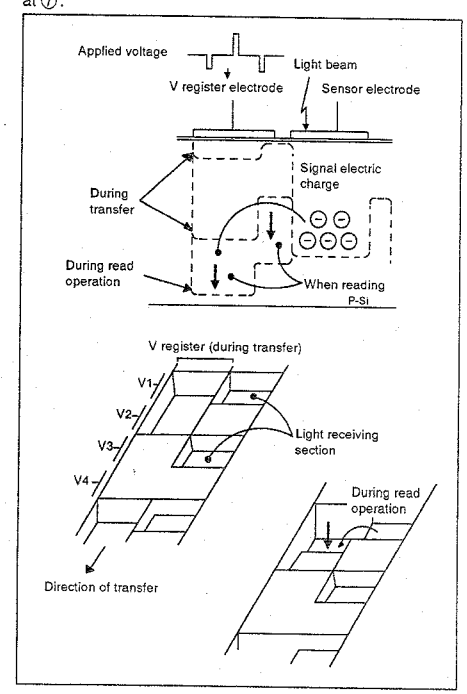


Fig. 2-4. 3-Value Drive Read

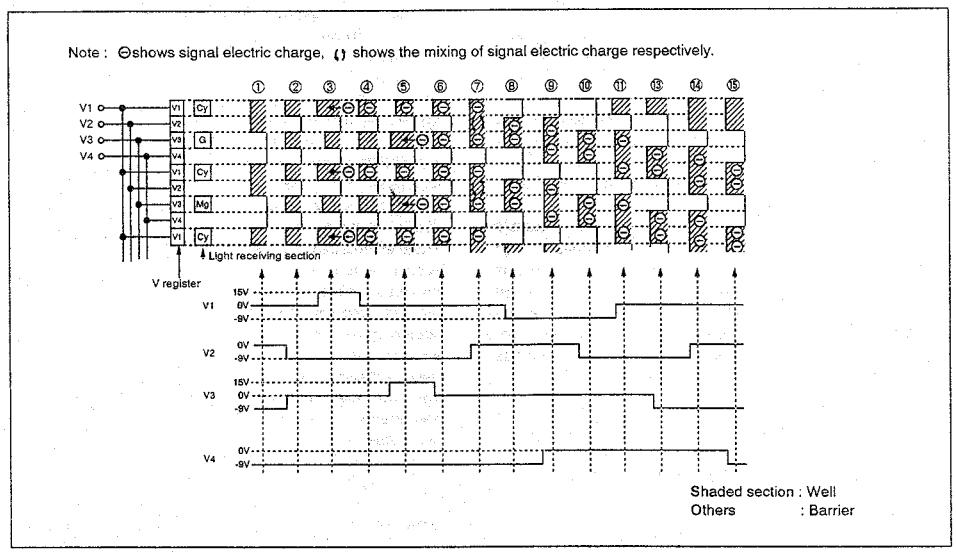


Fig. 2-5. CCD Sensor Read Timimng (Odd Field)

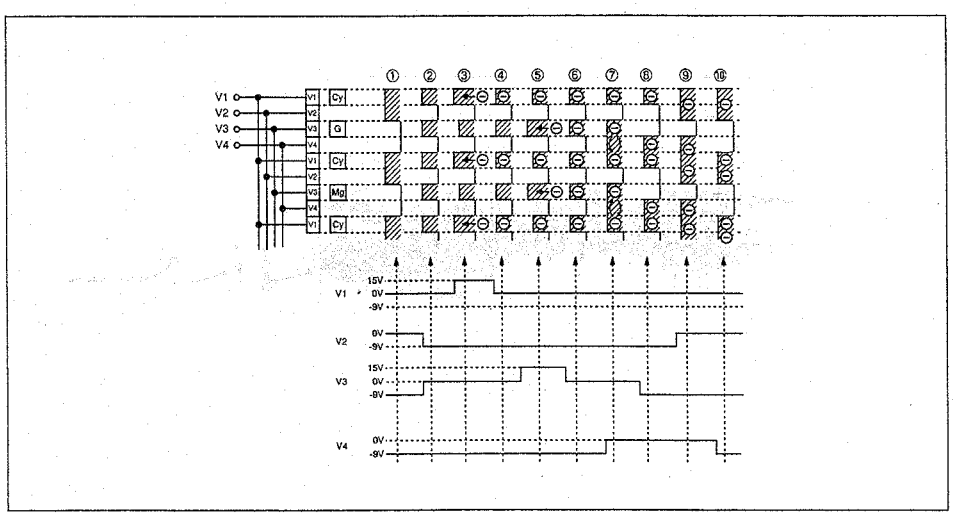


Fig. 2-6. CCD Sensor Read Timing (Even Field)

2-1-4. Transfer of Electric Charge by V Register

The H register makes the middle H1 a low potential during H blanking and is placed in a state of waiting for a signal from the V register, as shown in Fig. 2-7.

On the other hand, during H scanning period the V register that has been stopped after making V1 and V2 low in potential, makes transfer operation for one line based on 4-phase drive such as ① to ⑨ in the figure during H blanking.

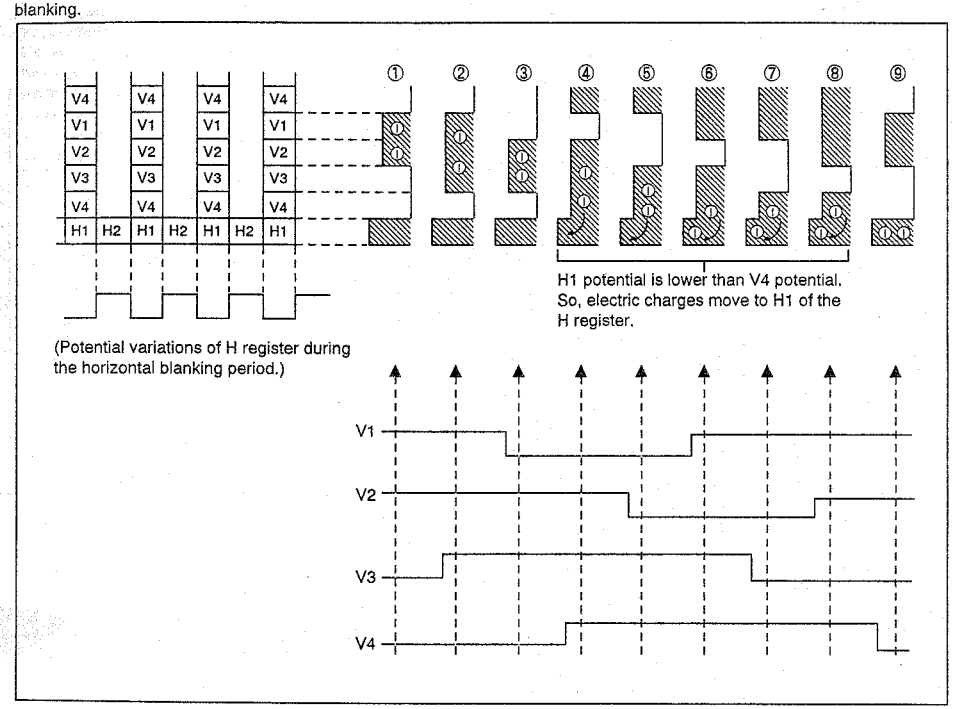


Fig. 2-7. Verticla Transfer of CCD and Applicatin of Electric Charge to the H Register

2-1-5. Transfer of Electric Charge by the H Register

Transfer system of H register employs 2-phase drive of simple drive circuit, since it enables to get larger area without limited by picture element as V register.

The electric charges sent to the final stage of the H register are transferred to the floating diffusion, as shown in Fig. 2-8. PG is turned on at the timing of (1), and the floating diffusion is charged to the potential of PD. At the timing of (2), the PG is turned off. In this condition, the floating diffusion is floated at high impedance. At the timing of (3), H1 potential becomes shallow, the electric charge now moves to the floating diffusion. Here, the electric charges are converted into voltages at the rate of V=Q/C by the equivalent capacitance C of the floating diffusion. And PG is turned on again at the timing of (1) by H1 potential when deep.

Thus, the potential of floating diffusion changes in proportion to the quantity of transferred electric charge, and became CCD output by receiving the source follower. The equivalent circuit of the output circuit is shown in Fig. 2-9.

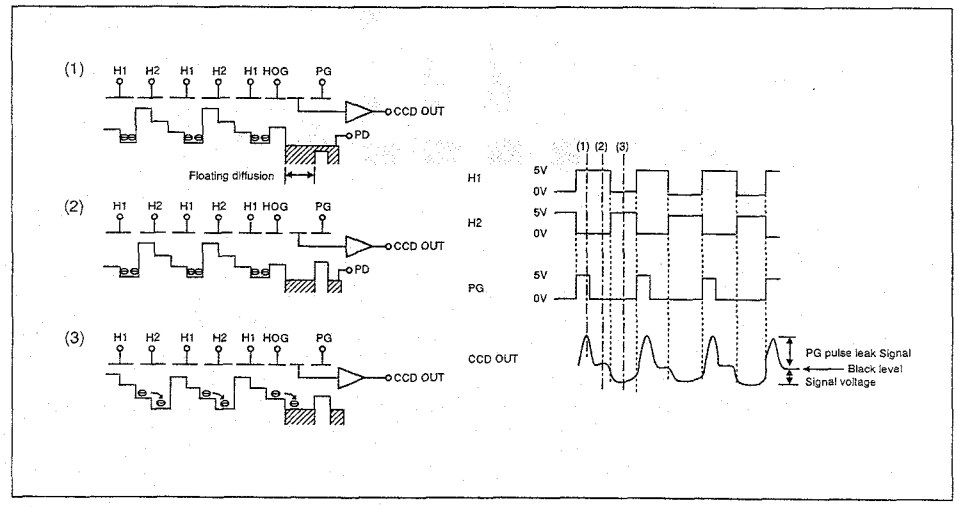


Fig. 2-8. Horizontal Transfer of CCD Imager and Extrction of Signal Voltage

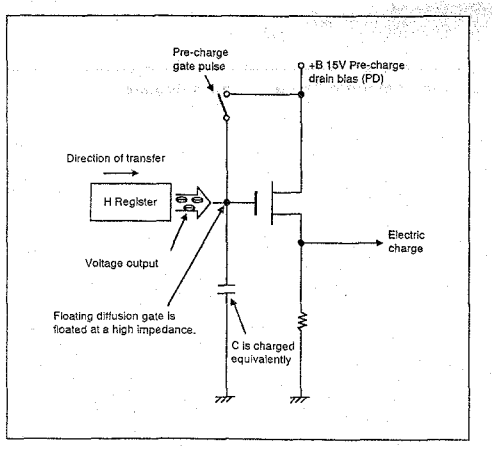


Fig. 2-9. Treory of Signal Extraction Operation

2-1-6. Vertical Overflow Drain (VOFD)

CCD of this system is configured as shown in Fig. 2-10. An imager which has OFD (SUB) provided in the vertical direction (in the direction of depth) of a CCD chip is referred to as the CCD of vertical overflow drain (VOFD) construction. When the potential along the dotted line (A–A') is seen from (a), it appears as (b). The height of the potential barrier is decided by applying DC bias to the OFD from outside. This is the same as determining the saturated electric amount Qs (equals to dynamic range) at the sensor.

Although the lager Qs are preferable, too large Qs cause a blooming, etc. (a phenomenon where the electric charge becomes too large, and leaks into other picture elements), and deteriorates the picture quality. Therefore, it is necessary to apply a well balanced DC bias.

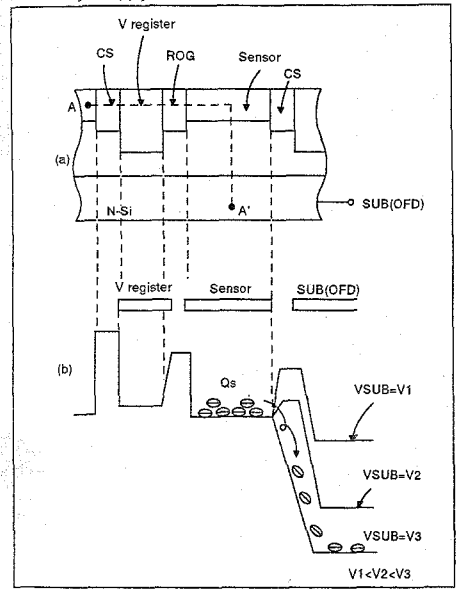


Fig. 2-10. VOFD and Potential Chart

2-1-7. Electronic Shutter

In normal operations, read-out from the signal charge can be made once in one field. Thus, the store time of the electric charge is 1/50 sec. However, by throwing away the electric charge during storing, the actual store time can be shortened. (Refer to Fig. 2-11.) The electronic shutter needs this kind of electric charge throwaway operation.

As shown in 2-1-6, in this system, the electric charge throwaway operation necessary for the electronic shutter is controlled by the DC bias applied to the OFD.

In other words, by setting the DC bias during the throwaway operation to the voltage V3 as shown in Fig. 2-10, the signal charge can be thrown away to the OFD. Actually, the throwaway operation is done during the horizontal blanking period in order to keep the picture from any noise that may appear during the throwaway operation. Under normal condition, the DC bias of the OFD is overlapped by an equivalent pulse of V1 to V2. (Refer to Fig. 2-12.)

In order to keep from any possible noise by the throwaway electric charge, the charge is distributed, and is not thrown away with only one pulse.

In theory, it is possible to control an electronic shutter with a store time of 1/50 sec to 1/15625 sec, in units of every 1/15625 sec interval by above system.

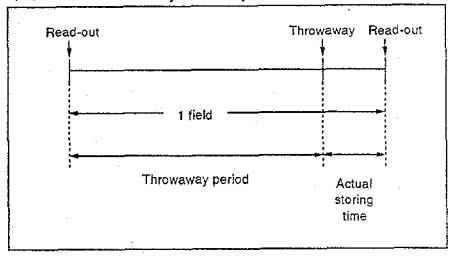


Fig. 2-11. Theory of Electronic Shutter

In this system a continuously variable speed shutter is used. The storing time is the time between the last fall of the pulse input to Pin ③ (Trig.) of IC916 from Pin ⑤ of the camera control microprocessor (IC932, TC1 Board), and the next read out pulse. (Refer to Fig. 2-12).

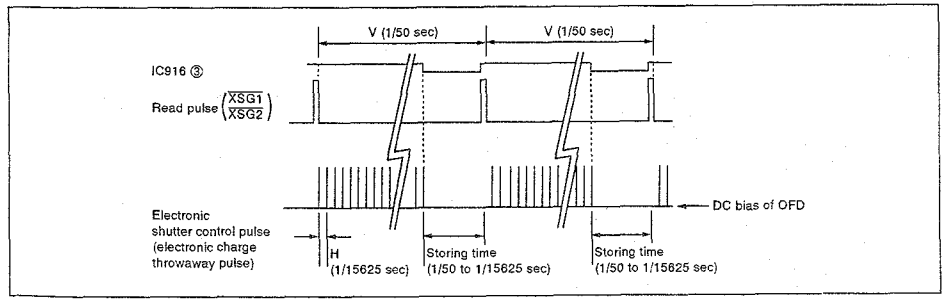

V (1/50 sec)
V (1/50 sec)
IC916 ③
Read pulse (XSG1 / XSG2)
Electronic shutter control pulse (electronic charge throwaway pulse)
DC bias of OFD
H (1/15625 sec)
Storing time (1/50 to 1/15625 sec)
Storing time (1/50 to 1/15625 sec)

Fig. 2-12. Actual Electronic Shutter Control

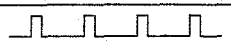
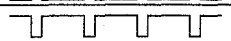
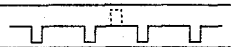
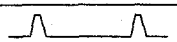
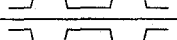
2-1-8. Terminal Voltage of CCD Imager

The terminal voltage of the CCD imager is given in Table 2-1.

In order to input a signal that has the specified timing and voltage for these terminals, the timing IC (IC916, CXD1253R) for generation of vertical and horizontal transfer clocks and PG clock and V driver IC (IC918, CXD1250N) are necessary. The block diagram is shown in Fig. 2-13.

XV1 to XV4 are the vertical transfer clock. In order to obtain a 3-value pulse, XSG1 and XSG2 are overlapped on XV1 and XV3. XSUB is the throwaway pulse for electronic shutter operations. H1 and H2 are the horizontal transfer clock, and PG is the pre-charged gate clock.

The pin assignment and the timing chart for the timing IC are shown in Fig.2-14 and Fig. 2-15.

Pin No.	Symbol	Pin Description	Waveform	Voltage
2	TP1	Input bias	DC	15V
3	V4	Vertical register transfer clock		-9V, 0V
4	V3	Vertical register transfer clock		-9V, 0V, 15V
5	V2	Vertical register transfer clock		-9V, 0V
6	V1	Vertical register transfer clock		-9V, 0V, 15V
7	GND	GND	GND	0V
8	V_{SS}	Output amplifier source	DC (self bias)	4V
9	V_{GG}	Output amplifier gate bias	DC	
10	OUT	Signal output		Approx. 10V
11	VDD	Output amplifier drain bias	DC	15V
12	VL	Protection transistor bias	DC	-9V
13	PG	Pre-charge gate clock		Adjustment value, adjustment value +5V
14	GND	GND	GND	0V
15	SUB	PCB (overflow drain) voltage	DC ( )*	Adjustment value (Adjustment value, adjustment value +24V)*
17	H1	Horizontal register transfer clock		0V, 5V
18	H2	Horizontal register transfer clock		0V, 5V
20	TP2	Input bias	DC	15V

( )* In the electronic shutter mode

Table 2-1. CCD Terminal Voltage

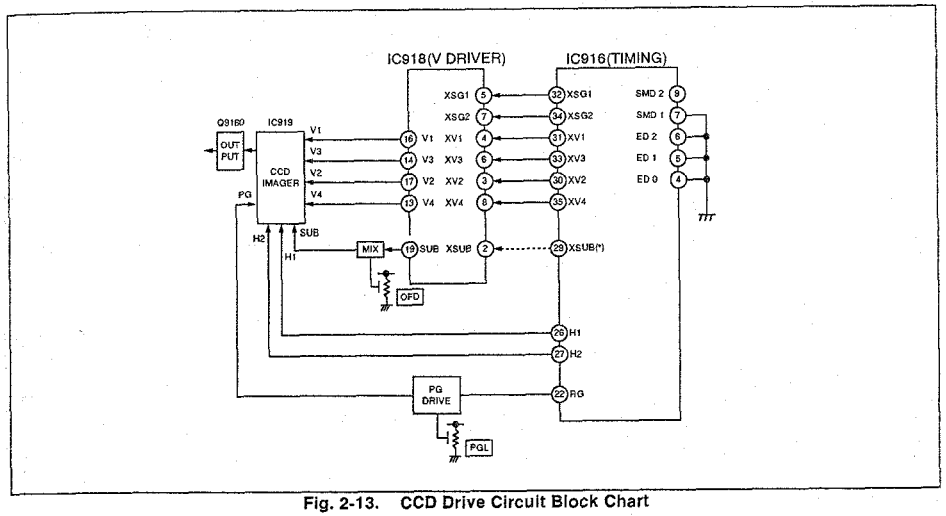


Fig. 2-13. CCD Drive Circuit Block Chart

Pin No. (VQFP)	Pin No. (QFP)	Pin Symbol	I/O	Pin Description
1	3	OSCOI	O	Inverter output terminal for oscillation
2	4	OSCI	I	Inverter input terminal for oscillation
3	5	TRIG	I	Continuous variable shutter control terminal(Pull-Up resistor)
4	6	ED0	I	Shutter speed control terminal (Mentioned later for details) (Pull-Up resistor)
5	7	ED1	I	
6	8	ED2	I	
7	9	SMD1	I	Shutter mode setting terminal (Pull-Up resistor) (Mentioned later for details)
8	10	Vss	–	GND
9	11	SMD2	I	Shutter mode setting terminal (Pull-Up resistor) (Mentioned later for details)
10	12	XVCT	O	Power control terminal of external ROM
11	13	D1	I	Data input terminal when using external ROM / When not using external ROM (Pull-Down resistor) / Normally "L"
12	14	D2	I	Normally "L"
13	15	D3	I	*1 / *2
14	16	D4	I	L: NTSC / H: PAL
15	17	A5	O	Address output terminal to external ROM
16	18	A4	O	
17	19	A3	O	
18	20	A0	O	
19	21	A1	O	
20	22	A2	O	
21	23	Vss3	–	GND
22	24	PG	O	Pre-charge gate pulse output terminal
23	25	NC	O	Should not be connected
24	26	VDD1	–	Power terminal
25	27	VDD2	–	Power terminal (for H1 and H2)
26	28	H1	O	Clock pulse output terminal for CCD horizontal register drive
27	29	H2	O	Clock pulse output terminal for CCD horizontal register drive
28	30	Vss2	–	GND (for H1 and H2)
29	31	XSUB	O	CCD electric charge throwaway pulse output terminal
30	32	XV2	O	Clock pulse output terminal for CCD vertical register drive
31	33	XV1	O	Clock pulse output terminal for CCD vertical register drive
32	34	XSG1	O	CCD sensor electric charge read out pulse output terminal
33	35	XV3	O	Clock pulse output terminal for CCD vertical register drive
34	36	XSG2	O	CCD sensor electric charge read out pulse output terminal
35	37	XV4	O	Clock pulse output terminal for CCD vertical register drive
36	38	TEST2	I	Should not be connected
37	39	MCK	O	Clock pulse output terminal for G3
38	40	XSHP	O	Pre-charge level • sample and hold pulse
39	41	XSHD	O	Data • sample and hold pulse
40	42	VSS1	–	GND
41	43	XSP1	O	Color separation sample and hold pulse
42	44	XSP2	O	Color separation sample and hold pulse
43	45	XSH1	O	Selection sample and hold pulse
44	46	XSH2	O	Selection sample and hold pulse
45	47	XDL1	O	Delay line clock (mosaic mode) /color separation sample and hold pulse(stripe)
46	48	XDL2	O	Delay line clock (mosaic mode) /selection sample and hold pulse(stripe)
47	49	BFG	O	Encoder • chroma modulator pulse. Defective address pulse when G3.
48	50	CLP1	O	Clamp pulse output terminal
49	51	CLP2	O	
50	52	CLP3	O	
51	53	CLP4	O	
52	54	PBLK	O	Pre-blanking cheaning pulse
53	55	ID	O	Line discriminating terminal (mosaic mode) : "L" (stripe mode)
54	56	WEN	O	Write enable terminal (only when low speed shutter)(Mentioned later for details)
55	57	GM	I	L : normal mode, H : G3 mode (pull-down resistor)
56	58	VDD1	–	Power terminal
57	59	CL	O	1/2 frequency-divided output terminal of the input clock from CK
58	60	PS	I	Electronic shutter speed data input L : serial input H : parallel input (pull-up resistor)
59	61	HD	I	Horizontal sync signal input terminal
60	62	VD	I	Vertical sync signal input terminal
61	63	HTSG	I	
62	64	TEST	I	Test terminal, L : normal mode, H : test mode (pull-down resistor)
63	1	XCK	O	
64	2	CK	I	Inverter input terminal for duty control (IC main clock input)

*1 ; L : Field accumulation
*2 ; H : Frame accumulation

Table 2-2. Timing IC Terminal Specification

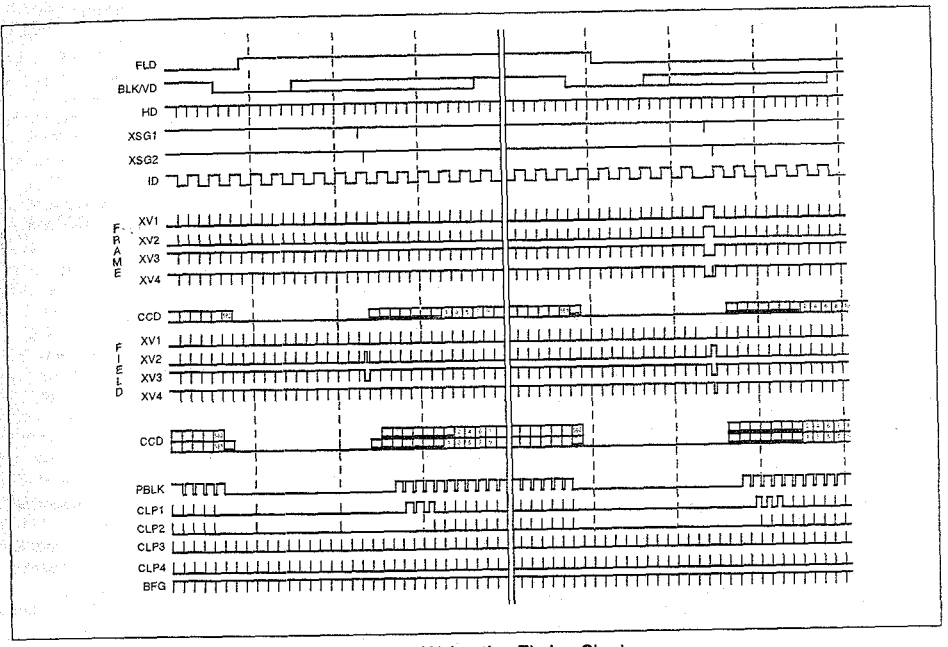


Fig. 2-14. V Direction Timing Chart

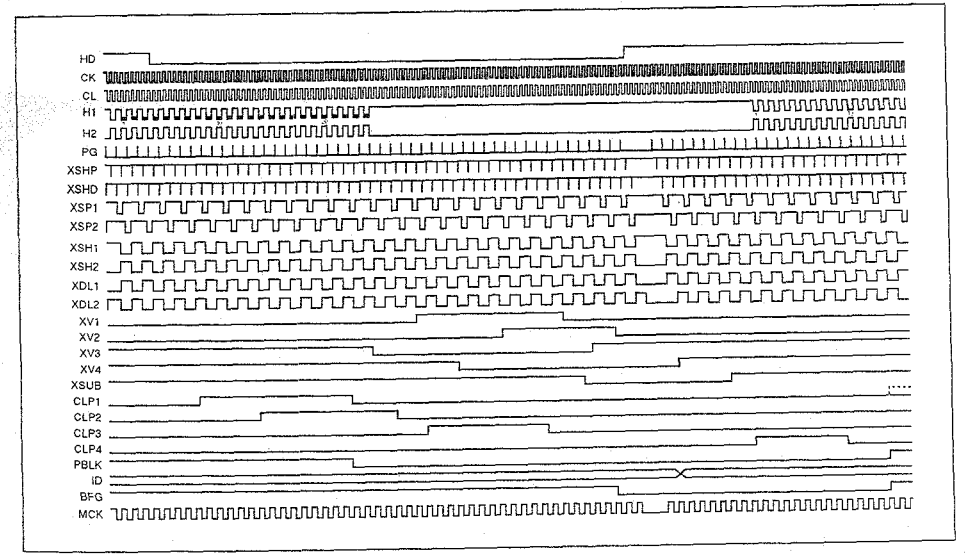


Fig. 2-15. H Direction Timing Chart

2-1-9. Shooting Method

The color filter arrangements that are used for the CCD in this system are shown in Fig. 2-16. The arrangement of 8 picture elements enclosed by bold line become one block. That block is lined horizontally and vertically. As described in 2-1-3, this system mixes 2 picture elements adjacent in vertical direction when reading signal charges. In other words, in Fig. 2-16, H1+H2, H3+H4...compose lines respectively that are read out. At this time, the signal compositions are as follows :

(H1+H2)line → Mg+Ye, G+Cy, Mg+Ye, G+Cy .....
(H3+H4)line → G+Ye, Mg+Cy, G+Ye, Mg+Cy .....
: : : :

And the same signal is repeated every 2 lines.
Here, draw an average of each line considering,
Mg=R+B, Ye=R+G, Cy=B+G :

(H1+H2)line → {(R+B+R+G)+(G+B+G)}/2=
(2R+3G+2B) /2
(H3+H4)line → {(G+G+R)+(R+B+B+G)}/2=
(2R+3G+2B) /2

By this, each line becomes the same value. In this system, by letting the CCD signal output pass through the LPF, each line is equalized, and is used for the luminance (Y) signal. Since the Y signal is proportional to 2R+3G+2B, B is reproduced brighter than reality, in comparison to the formula y (=0.3R+0.59G+0.11B) used in the specification for the television. But that is not a problem for actual usage.

On the other hand, since each line repeats the same signal every 2 picture elements, it is the equivalent of a conversion at the rate of the special frequency of the 2-picture element cycle (in this system, 4.77 MHz).

When seeking the level difference of the neighboring picture elements of the modulated component with the BPF or the sample hold, it becomes ;

(H1+H2)line → {(R+B+R+G)-(G+B+G)}=2R-G
(H3+H4)line → {(G+G+R)-(R+B+B+G)}=G-2B

Thus, 2R-G and G-2B components can be gained every 2 lines respectively.

In this system, this is used as the chroma (C) signal. However, it is impossible to get each r, g, b component required to create the chroma signal. Therefore, the un-obtained chroma signals are compensated by the signals taken from 1 line before. For example, in (H3+H4) line, each component of r, g, b can be obtained by 2R-B of (H1+H2) line. Therefore, 1H delay line is absolutely necessary to this system. At the same time, in order to obtain r, g and b, from 2R-G and G-2B, the following formulas are used.

r → (2R-G)+0.12Y=2.24R-0.64G+0.24B
g → Y-(2R-G)+(G-2B)=5G
b → -(G-2B)+0.2{Y-(2R-G)}=2.4B-0.2G
(However, when Y=2R+3G+2B)

Both r and b are mixed with other chroma components, but there is no problem in its actual usage.

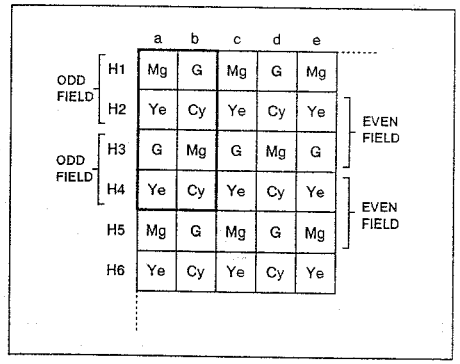

a b c d e
ODD FIELD
H1 Mg G Mg G Mg
H2 Ye Cy Ye Cy Ye
EVEN FIELD
ODD FIELD
H3 G Mg G Mg G
H4 Ye Cy Ye Cy Ye
EVEN FIELD
H5 Mg G Mg G Mg
H6 Ye Cy Ye Cy Ye

Fig. 2-16. Color Filter

2-2. IC CONFIGURATION

This system mainly consists of following IC.

IC919 (ICX045)	CCD imager
IC917(CXA1390R)	CDS, AGC and color separation, etc.
IC914(CXA1391R)	Gamma correction, chroma synchronization, white balance, matrix, etc.
IC912(CXA1392R)	Balanced modulator, aperture correction, etc.
IC913(CXL1508N)	Narrow band 1H delay line × 3

And, ICs required for above IC function

IC918(CXD1250N)	V driver
IC916(CXD1253R)	Timing pulse generator
IC915(CXD1217Q)	Sync signal generation
IC911(MSM6524GS)	Electronic volume

2-3. IC917(Fig. 2-17.)

2-3-1. CDS Circuit

The video signal output from the CCD is input to Pin ㊲ and Pin ㊳ of IC917. Inside, there are five sample/hold circuits originating in the XSHP and XSHD pulses, and there perform the CDS (Correlated Double Sampling). The objective of the CDS is to eliminate noise components from the CCD output, and extract the effective signal components in the highest possible S/N status. This is described in Fig. 2-18. As shown in Fig. 2-8, the CCD output includes black level information and signal component, and a noise effected by a leak of the harmful PG clock.

In CDS, the black level is detected by the S/H of the XSHP (Fig. 2-18 Ⓐ), and the signal components are detected by the S/H of the XSHD (Fig. 2-18 Ⓒ). An effective signal component can be obtained through Ⓒ - Ⓐ, but these signals would include noise effected by the drain of S/H pulse, and would decrease the S/N ratio. Here, by performing S/H through the XSHD again in Ⓐ, it becomes Ⓑ, and the phase of the noise created by the drain and Ⓒ can be combined.

By the signal obtained from Ⓒ - Ⓑ, a signal component Ⓓ with the noise eliminated can be obtained. Fig. 2-17 shows the XSHP performing S/H once again. This is to perform a finer elimination of the noise.

Next, the CDS output is input to the AGC amplifier and high luminance detection circuit. And the CDS output is fed from Pin ⑰ to the auto iris circuit (Q9322 Pin ②) and auto focus circuit (Q9301 Pin ②) after passing through gain control circuit to clamp and blanking circuits.

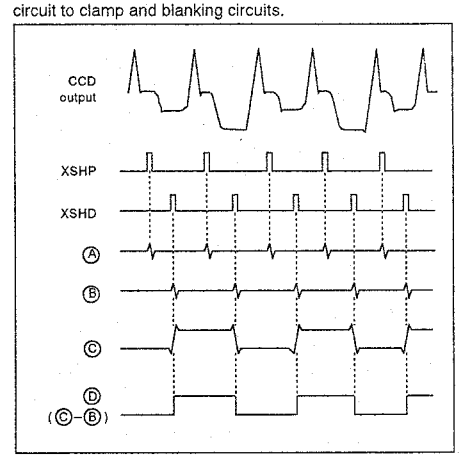


Fig. 2-18. CDS Circuit

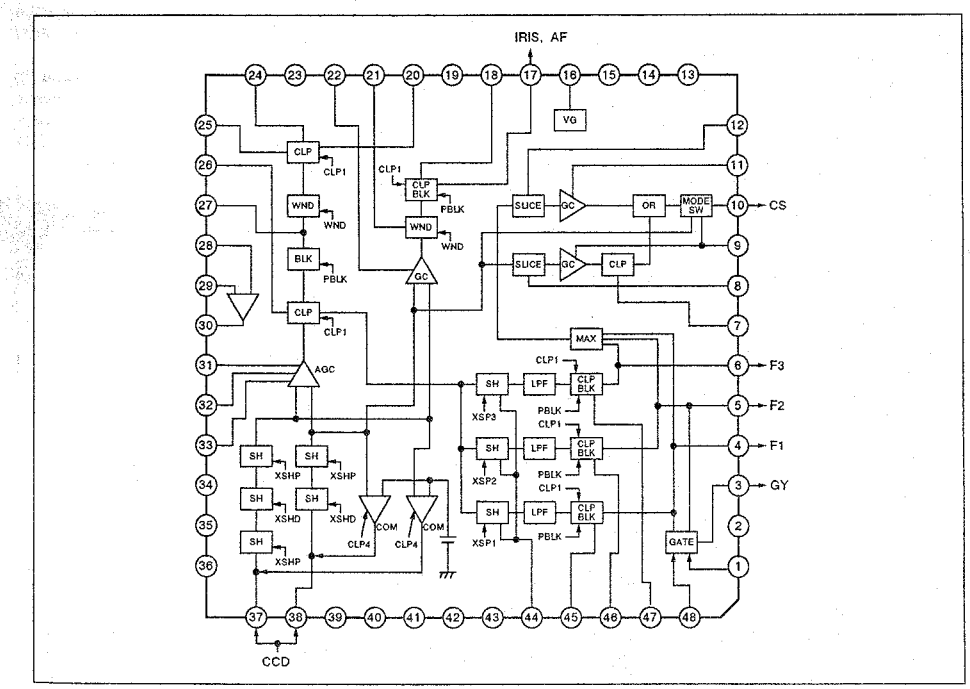


Fig. 2-17. IC917 Block Diagram

2-3-2. AGC Circuit

This circuit controls gain so that the outputs of AGC amplifier level become constant. The AGC circuit amplifies the gain approximately 18 dB under the minimum illumination condition. AGC level, determined by the reference voltage of Pin ㉘, is adjusted by the voltage at Pin ⑤ of IC911 then AE corrected by PWM output of Pin ㊹ of IC932.

2-3-3. High Luminance Detect Circuit

In high luminance detection circuit, a signal sliced the sample and hold output by XSHD is added to a signal sliced the maximum value of F1, F2 and F3 (mentioned later) in the light amount that the most sensitive color filter of CCD is saturated, then the signal is fed from ⑩ to IC914 as CS signal. This signal prevents that a green coloring phenomenon which occurs when the signals are saturated and the linearity in the chroma modulation becomes deficient.

2-3-4. Color Separation Sample and Hold Circuit

AGC amplifier output is input into the color separation sample and hold circuit. Since XSP1 and XSP2 are 4.73 MHz sampling pulses with phase difference of 180°, continuous F1 and F2 signals of 2 picture elements cycle can be extracted. Fig. 2-19. shows these relations. F1 and F2 are chroma signals with G+Cy (Mg+Cy), Mg+Ye (G+Ye) components respectively. ( ) shows 1H delayed signal. After passing through the LPF to eliminate the excess high frequency components, F1 and F2 are output from Pins ④ and ⑤ via clamp and blanking circuits.

On the other hand, the XSP3 (Pin ㊵) of IC917 is grounded and the AGC output is passed through LPF, clamp, pre-blanking circuits to Pin ⑥. As for F1 and F2, sample and hold (S/H) is performed in the GATE block shown in Figs. 2-19(b) and (c), and the GY signal is composed and output from Pin ③. By passing through the GATE block, approximately 160ns of delay can be performed. After the excess high frequency component and the 4.73 MHz component are eliminated by T9190, GY signal is fed to Pin ㊸ of IC914 as high frequency luminance signal.

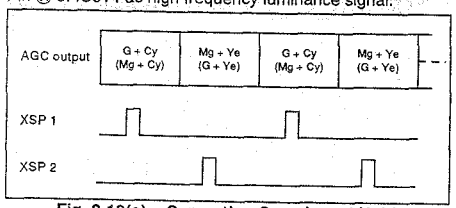


Fig. 2-19(a). Separation Sample and Hold

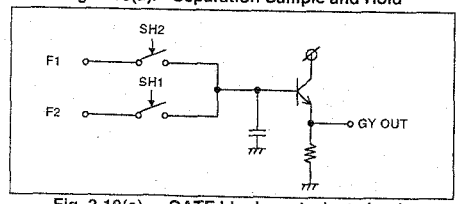


Fig. 2-19(c). GATE block equivalent circuit

2-4. IC913 AND IC914 (Fig. 2-20)

2-4-1. Chroma Synchronization

The chroma separated outputs F1 and F2 are fed through Pins ㊾ and ㊿ of IC914. As mentioned in 2-1-9, difference between F1 and F2 becomes a signal (C_o) in which (2R-G) and (G-2B) are appeared alternately every two lines. C_o is fed from Pin ㊻ to Pin ㉓ of IC913. IC913 contains three channels of narrow band 1H delay line driven by two clocks (XDL1 and XDL2 of 4.73 MHz) phase shifted by 180°.

Signal C_1 created by 1H delayed C_o is again input to Pin ㊽ of IC914. C_o and C_1 are synchronized by MPX after passing through LPF and creates continuous 2R-G and G-2B. (See Fig. 2-21.)

C_1 level is adjusted by the voltage of IC911 (Pin ③) so that continuous 2R-G and G-2B signals have no level difference by every 1H.

On the other hand, after F1 and F2 are added, the signal passes through the clamping circuit and LPF and is used as a narrow band luminance signal Y_o. Y_o is used for RGB matrix and V aperture circuits.

2-4-2. V Aperture Circuit

Y_o and Y_1 signals pass through LPF, KNEE (white compression), 2H aperture control, LPF, clamping circuit, slicer (noise reduction) and GC, resulting in V aperture signal (VAP) creation.

2H aperture control circuit calculates $Y_o - Y_1$ as shown in Fig. 2-22. VAP is fed from Pin ⑪ of IC914 to Pin ㊷ of IC912.

In order to eliminate the pseudo signal generated at vertical edge section, VAP is added to high luminance detect signal (CS) created by IC917, after passing through the absolute value circuit (ABS), then fed from Pin ㉔ to IC912 as chroma suppression signal (CSY).

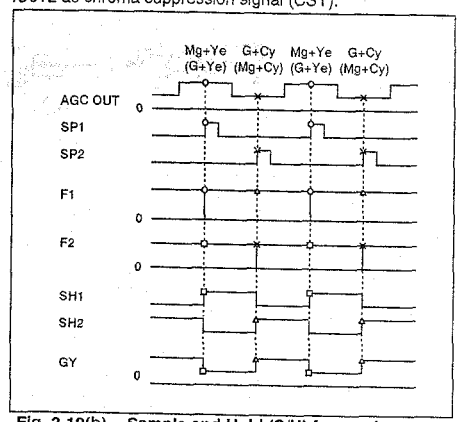


Fig. 2-19(b). Sample and Hold (S/H) from color separation to GY composition

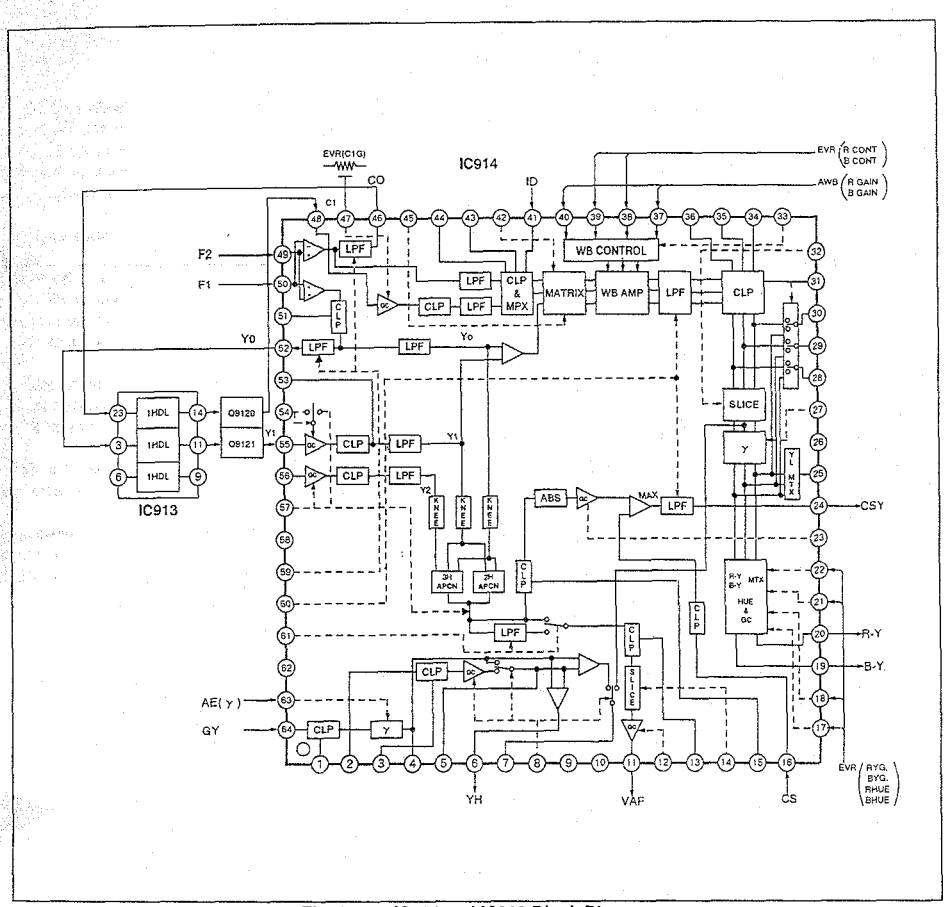


Fig. 2-20. IC914 and IC913 Block Diagram

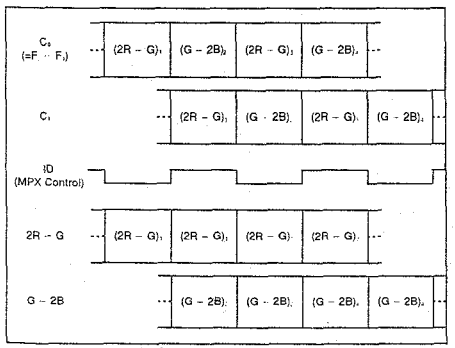


Fig. 2-21. Chroma Synchronization (MPX)

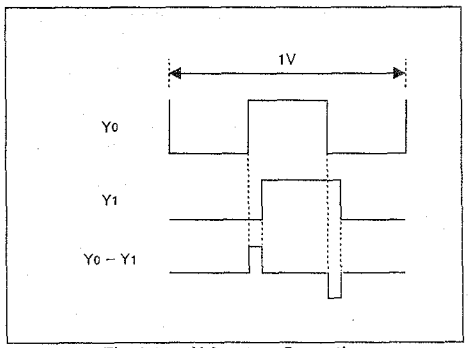


Fig. 2-22. V Aperture Correction

2-4-3. White Balance • Matrix • Gamma Compensation

The 2R-G and G-2B signals obtained by MPX are calculated with Y ($=Y_e+Y_i$) and generates the r, g and b signals as mentioned in 2-1-9. Later on, it adjusts the white balance. Adjusting the white balance means shooting a white subject, the r and b levels are controlled so that the chroma signals after subcarrier modulation become zero.
In fact, it is controlled to become ;

r=g and b=g.

White balance is adjusted by the voltage of Pin ⑬ and ⑯ of IC911 and VR931 and VR932, and automatically controlled by PWM output of Pin ② and ③ of IC932.
The r, g and b signals after white balance compensation is limited to the bandwidth required for the chroma signal by LPF and low level noise component is eliminated by the slicing circuit, then appropriate gamma compensation is performed by the gamma (γ) circuit.
In R-Y and B-Y matrix, HUE and GC circuits, R-Y and B-Y is created using r, g and b signals gamma compensated, and hue adjustment is done by HUE circuit using following formulas :

$(R\text{-}Y)' = (R\text{-}Y) \pm \alpha\,(B\text{-}Y)$
$(B\text{-}Y)' = (B\text{-}Y) \pm \beta\,(R\text{-}Y)$

The GC circuit adjusts each level of (R-Y)' and (B-Y)'.
The hue and level are adjusted by the voltage of Pins ⑩, ⑫ ⑧ and ⑨ of IC911.

2-4-4. YH Processing

The GY signal (YH) fed to Pin ⑭ of IC914 is clamped and compensated for proper gamma. Gamma characteristic is determined by the voltage of Pin ⑬. The signal is AE corrected by PWM output of Pin ⑬ of IC932.
The gamma compensated YH is output from Pin ⑥.

2-5. IC912 (Fig. 2-23)

2-5-1. Y Signal Processing

The YH signal passed through Q9070, Q9071 is fed to Pin ㉟ via DL for H aperture correction (T9020, delay time t=approx. 150 nsec) at 1kΩ if output impedance. Since DL is terminated at high impedance, reflection wave is generated as shown in Fig. 2-24. and superimposed into YH (Pin ㉝).
Pins ㉝ and ㉟ are differential amplified inside of IC and become H aperture signal (HAP).
HAP level is given by the voltage at Pin ㊱. The level is suppressed by the increase of AGC voltage at Pin ㉛ of IC917 when AGC gain is high. After slicing the low level component, the HAP signal is added to Y signal of Pin ㉟ and VAP signal of Pin ㊷.
Thus, the aperture corrected Y signal is gain adjusted by the voltage of Pin ⑥ of IC911, and the attenuation level is determined by the FADE control voltage simultaneously input to Pin ㉘.
The output of Y level becomes 100% when the FADE control voltage is 0V, is attenuated when 2V or more and becomes 0% when 2.9V or more.
The Y signal is added with setup level that is adjusted by Pin ⑤ of IC911, is passed through the white clip limiting high luminance, then fed from Pin ㉒ to the VTR as CAM.Y with sync signal added.

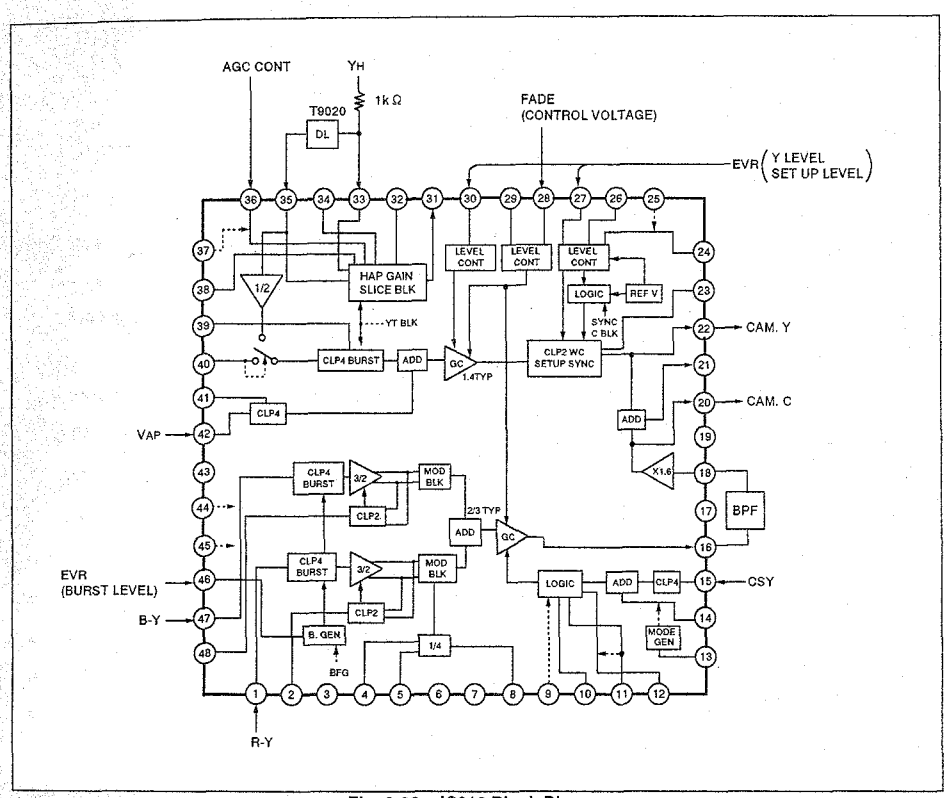


Fig. 2-23. IC912 Block Diagram

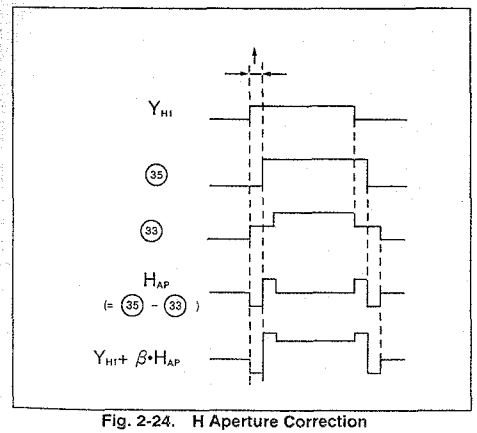


Fig. 2-24. H Aperture Correction

2-5-2. C Signal Processing

The R-Y and B-Y signals from Pins ① and ㊼ are clamped, added with burst flag pulse, and passed through the subcarrier modulation and blanking circuits, respectively, then level controlled at GC block after added each other.
In GC block, the C signal is once output from Pin ⑯ after suppressed at high luminance section and vertical edge by CSY (Pin ⑮), suppressed at low illumination by AGC voltage (Pin ⑭) and attenuated by FADE voltage as Y signal. After band limited by the external BPF. the C signal is input to Pin ⑱ again, and fed from Pin ⑳ to the VTR as CAM.C after amplified.

2-6. IC915

Pin ⑤ of IC915 receives 14 MHz clock from Pin ㊼ of IC916 and generates various sync signals. The block diagram, timing chart and Pin function are shown in Fig. 2-25, 2-26 and 2-27, and Table 2-4 respectively.

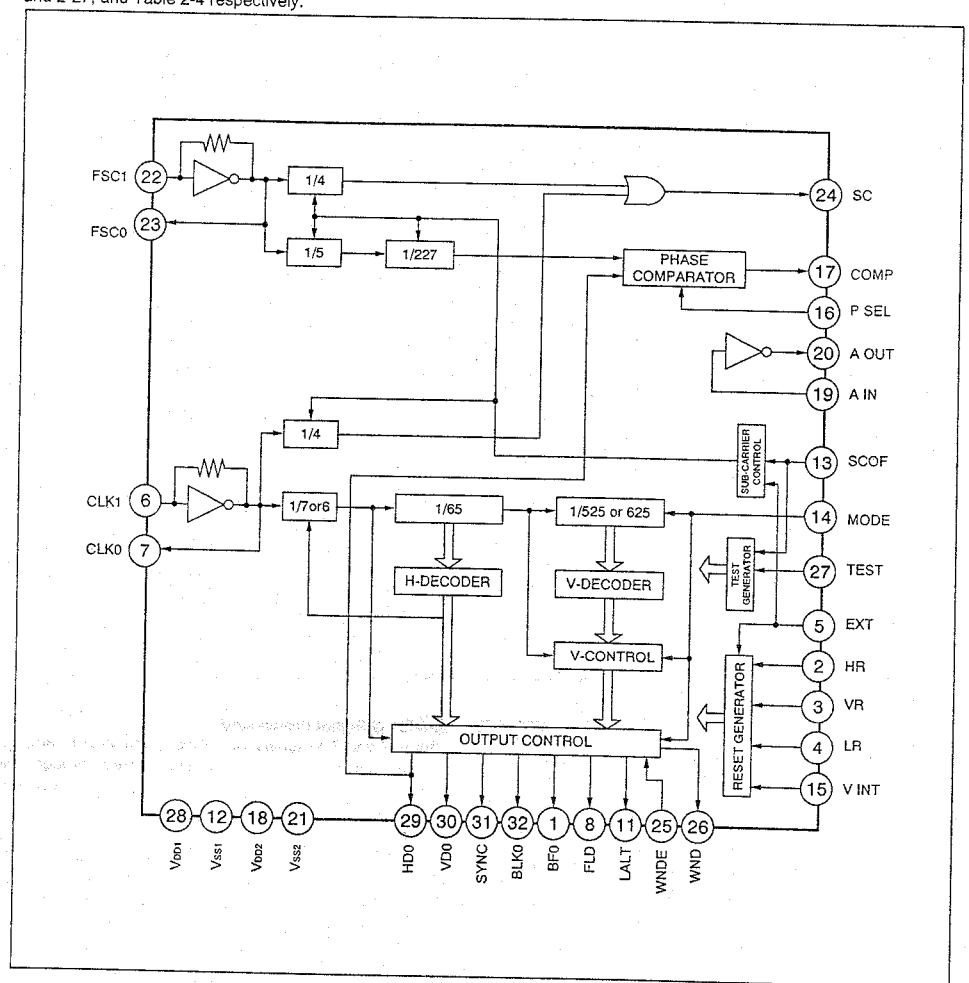


Fig. 2-25. IC915 Block Diagram

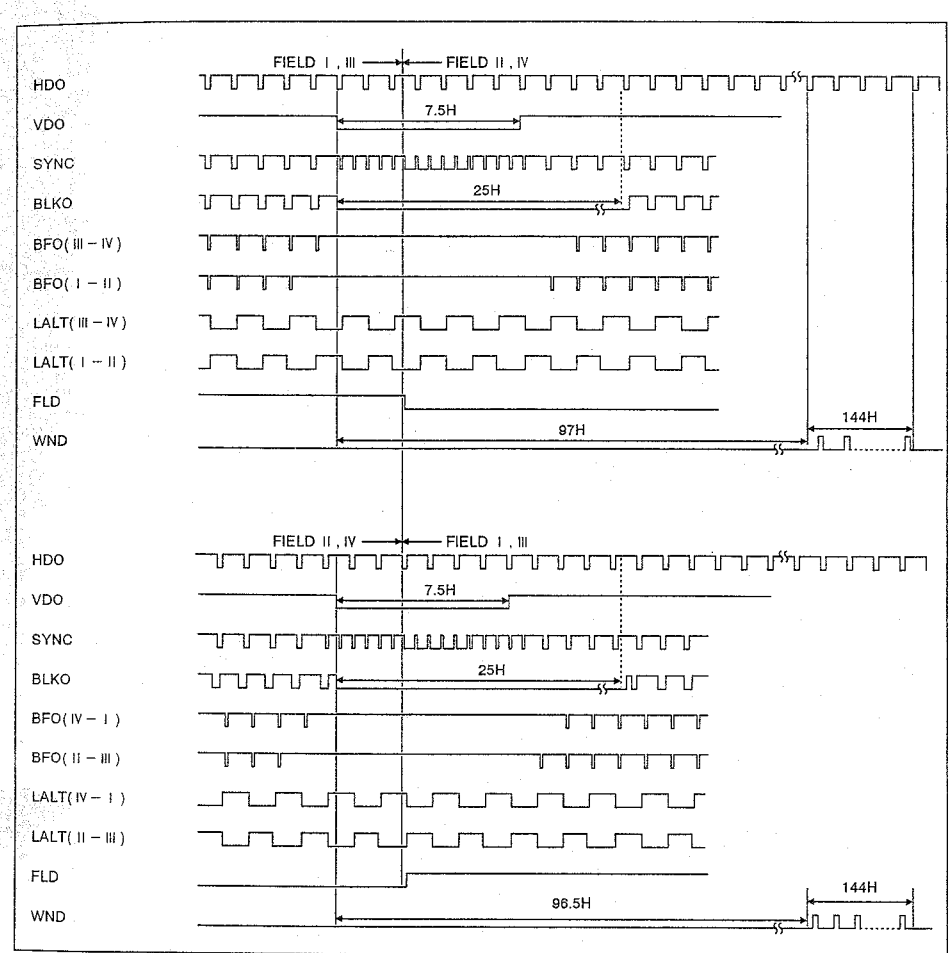


Fig. 2-26. V Direction Timing Chart

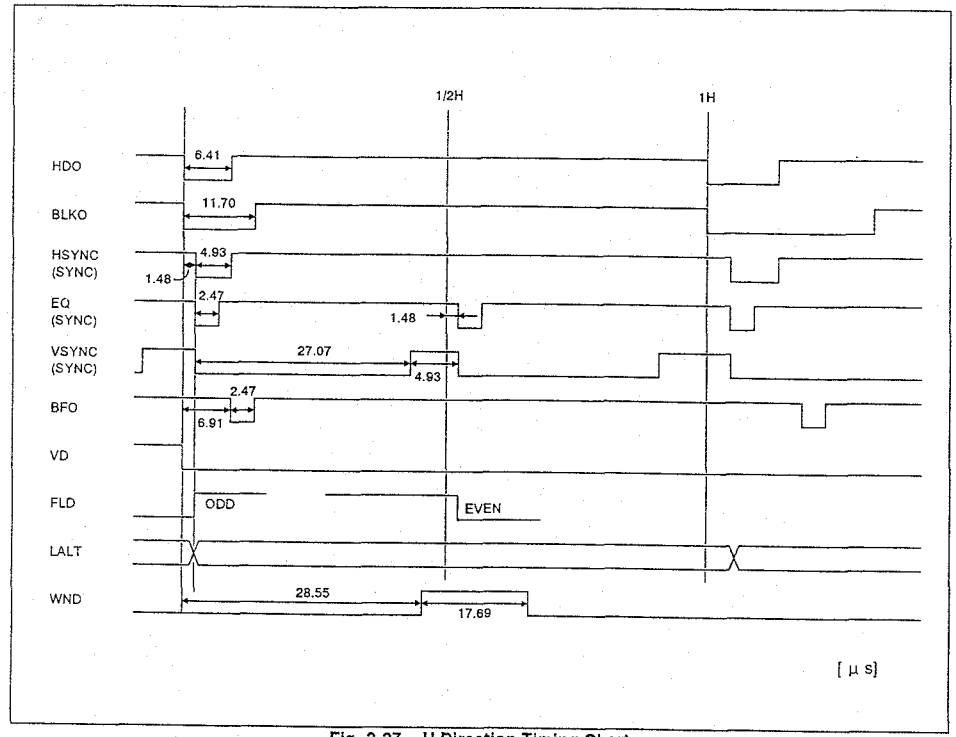


Fig. 2-27. H Direction Timing Chart

Pin No.	Pin Symbol	I/O	Pin Description
1	BFO	O	Burst flag pulse
2	HR	I	Horizontal reset input
3	VR	I	Vertical reset input
4	LR	I	Line selection reset input
5	EXT	I	Internal / external ($\overline{INT}$ / EXT) mode selection
6	CLKI	I	Clock input (NTSC : 14.31818MHz, PAL : 14.1875MHz)
7	CLKO	O	Clock output
8	FLD	O	Field pulse
9	N. C.		
10	N. C.		
11	LALT	O	Line selection output (Line alternator pulse)
12	V_{SS1}		GND
13	SCOF	I	Sub-carrier suppressed input L : OFF
14	MODE	I	NTSC / PAL mode selection ($\overline{NTSC}$ / PAL)
15	VINT	I	Initialize input
16	PSEL	I	Phase comparator polarity selection
17	COMP	O	Phase comparator output
18	V_{DD2}		Filter invertor +5V
19	AIN	I	Filter invertor input
20	AOUT	O	Filter invertor output
21	V_{SS2}		Filter invertor GND
22	FSCI	I	4 fsc clock input
23	FSCO	O	4 fsc clock output
24	SC	O	Sub-carrier output
25	WNDE	I	Window output enable input (Enabled at "L")
26	WND	O	Window output
27	TEST	I	Test input (normal "L")
28	V_{DD1}		+5V
29	HDO	O	Horizontal drive pulse
30	VDO	O	Vertical drive pulse
31	SYNC	O	Composite synchronous pulse
32	BLKO	O	Composite blanking pulse

Table 2-4. IC915 Pin functions

2-7. IC911

IC911 is a serial input IC which is built 96-bit EEPROM and 12-channel D/A converter, and converts data non-volatile stored at EEPROM into analog voltage to output.
IC911 is built the auto load function that automatically loads the whole contents of EEPROM and automatically sets the D/A converter output when power is turned ON.
When adjusting, IC911 communicates with the adjustment controller for service. The block diagram and Pin function are shown in Fig. 2-28 and Table 2-5 respectively.

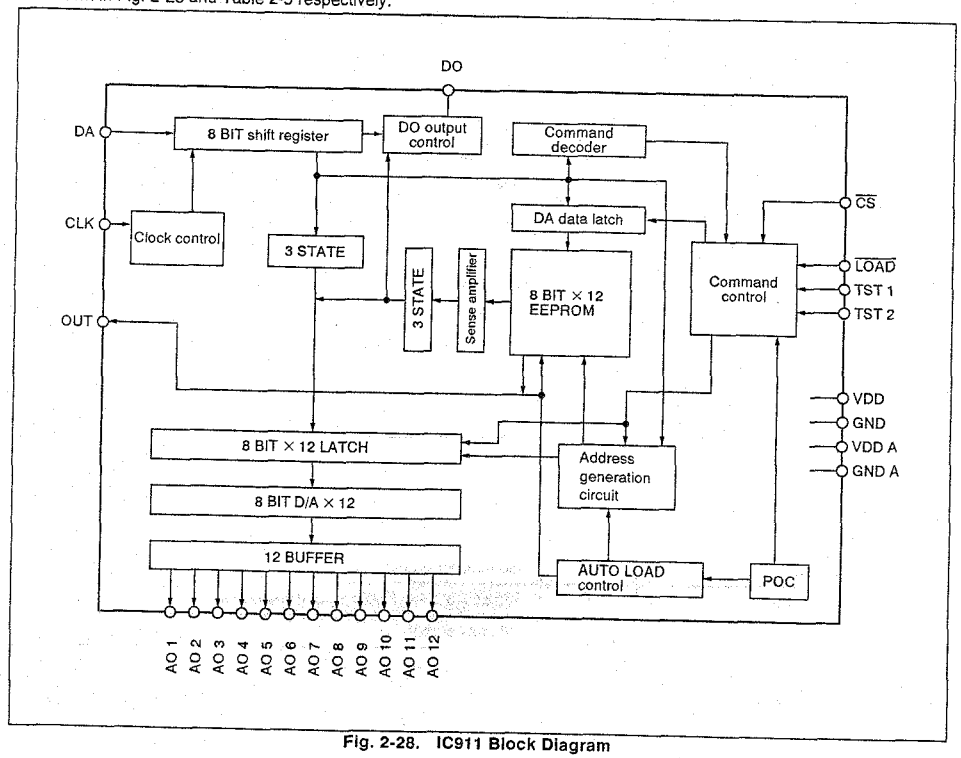


Fig. 2-28. IC911 Block Diagram

Pin No.	Pin Symbol	I/O	Pin Description
1	GNDA	–	Analog GND
2	AO2	O	8 bit D/A output
3	AO3	O	
5	AO4	O	
6	AO5	O	
7	AO6	O	
8	AO7	O	
9	AO8	O	
10	AO9	O	
12	AO10	O	
13	AO11	O	
14	VDDA	–	Analog power
15	V_{DD}	–	Logic power
16	AO12	O	8 bit D/A output
17	TST2	I	Test terminal 2
19	TST1	I	Test terminal 1
20	OUT	O	Monitor terminal
21	D_O	O	Outputs LSB bit data of 8 bit shift register.
22	$\overline{LOAD}$	I	Load pulse input terminal to load data of 8 bit shift register to latch.
23	DA	I	Serial data input terminal Inputs LSB first 8 bit data.
24	CLK	I	Shift clock input terminal. Input signal of DA terminal of 8 bit shift register at shift clock rising.
26	$\overline{CS}$	I	White mode protect terminal
27	AO1	O	8 bit D/A output
28	GND	–	Logic GND

Table 2-5. Terminal Specification

2-8. DIGITAL AF OPERATION

2-8-1. Digital AF Principle

This system digital integrates the high band component contained in video signal (performs multiplication and addition in every vertical period : hereafter referred to as evaluation value) and controls the focus motor by 8-bit microprocessor so that the integrated value becomes maximum.

The charge of AF evaluation value when lens position is moved for common object is shown in Fig. 2-29. In basic operation of this system, the focus lens is controlled by the motor so that AF evaluation value is always increased.

When AF evaluation value is decreased (the maximum value of the evaluation curve is identified), the focus motor is operated in reverse direction and the focus lens is returned and stopped to a position where the maximum value of the evaluation curve is identified.

After that, according to the change of object information (the form of the curve of evaluation value is changed and the current position is not a summit of the curve.), microprocessor monitors the lens position so that it always searches a summit of the evaluation curve.

2-8-2. Initial Operation at Power Turning ON

When power is turned ON, the focus lens is once moved up to the point at which the focus position sensor switches, then AF and other operations are started. (The position of the focus lens is stored in the microprocessor by this operation.)

If the focus motor or focus position sensor is defective, AF, zoom or high speed shutter will not operate at all.

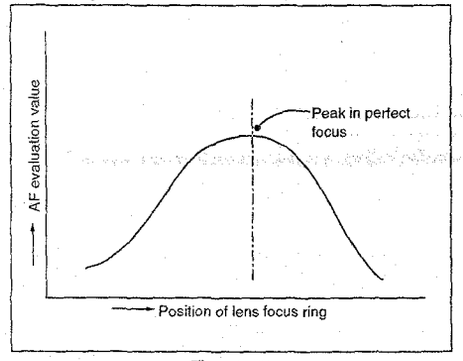


Fig. 2-29.

2-8-3. Operation Instruction

IRIS signal output from Pin ⑰ of IC917 (CA1 Board) is amplified by Q9302 after increase the low luminance component by Q9301. (TC1 Board)

The signal is divided into signals of mote than 200 kHz and more than 600 kHz by Q9304 and input to Pins ㉞ and ㉟ of the standard cell. These signals are selected together with AE signal mentioned later by the standard cell, then output to Pin ㊿.

These time shared multiplex signals are band limited to 2.4 MHz by LPF of L9303, C9361 and C9362 via the buffer amplifier of Q9309, then peak held by Q9308 and Q9329. After which the signal is converted into digital signal by A/D converter in the standard cell and integrated in every area as shown in Fig. 2-30.

Integrated AF evaluation value is fed to IC932 of microprocessor and AF operation is done based on AF evaluation value of focus zones 1 and 2. The selection of these focus zones is determined by fuzzy theory of microprocessor and controlled so that focused on the object center of the screen. IRIS DRIVE signal is fed from IC935 to Pin ㊲ of the standard cell and changes AF operation according to the iris condition.

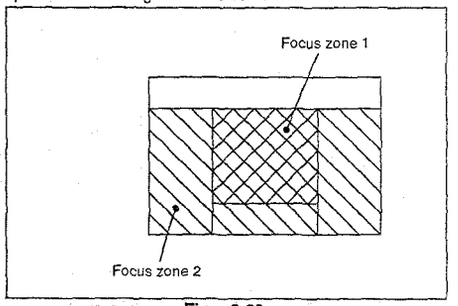


Fig. 2-30.

2-8-4. When AF Operation Won't Track, or Cannot Move Smoothly

① Object outside of focus zone for calculating the evaluation value
This system only obtains evaluation value calculation information within the focus zones (see Fig. 2-30) and ignores object outside of focus zone.

② Extremely low evaluation value
- Poor S/N ratio under low illumination condition
- No contrast on object

③ Sudden zooming operation
- Objects moving violently, or too fast severe panning or tilting of camera
- Severe hand movement

④ Object within 1.1 mm focus length can not be focused structuralily with tele-zooming.

2-9. INNER FOCUS SYSTEM

The inner focus is controlling focus by moving lens of the most back side of lens system. Compared with the conventional front focus method, this system features are below:

1) Focusing can be done from approximately 10 mm to infinity.
2) A compact and light weight focus lens can realize rapid focusing.
3) Since peripheral light amount can be obtained (shooting in short distance) without increasing the front lens diameter, a compact and light weight can be realized.

2-10. DIGITAL AE (AUTO IRIS)

This system can be controlled the counter light or excessive light condition by controlling iris, AGC and gamma level based on the luminance level of each of six video areas.

IRIS signal is fed from Pin ⑰ of IC917 (CA1 Board) to Pin ㊵ of IC931 (TC1 Board) of the standard cell and clamped by a voltage at Pin ㊶. After which, AE process is done at certain time (1V) by time sharing system with AF.

At this time the signal is A/D converted and integrated every area by the standard cell, and become amount (evaluation value) indicating the luminance level of each area. Microprocessor IC932 receives evaluation value at the same timing as AF and judges counter light or excessive light condition using fuzzy theory based on characteristics that most objects is placed center of the frame. This determines the compensation value of iris, AGC and gamma level to output to Pins ㊹ and ㊸ (as PWM data).

IRIS signal is detected by Q9322 and input to Pin ⑥ of IC935, then compared with the reference voltage input to Pin ③ to drive the iris coil by the voltage difference.

The PWM output of Pins ㊹ and ㊸ of microprocessor and become IRIS REF, AGC REF and gamma CONT signals.

With Pin ⑧ of CN915 is in "L", the digital AE function is turned OFF and results in standard condition where each compensation is not done.

2-11. AWB (AUTO WHITE BALANCE) CIRCUIT

In AWB circuit, picture frame is divided into 8 areas in vertical and horizontal direction respectively (total of 64 areas) and the video information of each area is analyzed by microprocessor, then the color of object is assumed and chroma compensation is performed. B-Y and R-Y signals from Pins ⑲ and ⑳ of IC914 (CA1 Board) pass through Q9021, are amplified by Q9331 and Q9332 of the TC1 Board, then input to Pins ㊺ and ㊸ of IC931 of the standard cell. They are clamped by a voltage at Pin ㊹ and A/D converted every 64 areas, then input to microprocessor.

The microprocessor analyses brightness information, color level, hue and area occupied by one color, etc. and determines the control amount of AWB circuit then resultant control voltages are sent to Pins ② and ③ of IC932.

The signals are input to Pins ㊵ and ㊲ of IC914 as B and R GAIN control signals to control white balance.

2-12. INTERNAL COMMUNICATION

The microprocessor IC932 is linked to the A/D convertor IC934, the EEPROM loaded in the lens, and to IC351 inside the system control block by a serial communication bus (SK, SO, SI) common to all of them. Selection of the object of communication is performed in the various ports for chip selection (Pins ⑦, ⑨ and ⑪ of IC932).

The input from the switches below is read inside the system control block then fed to the microprocessor IC932 by the above mentioned serial communication method.

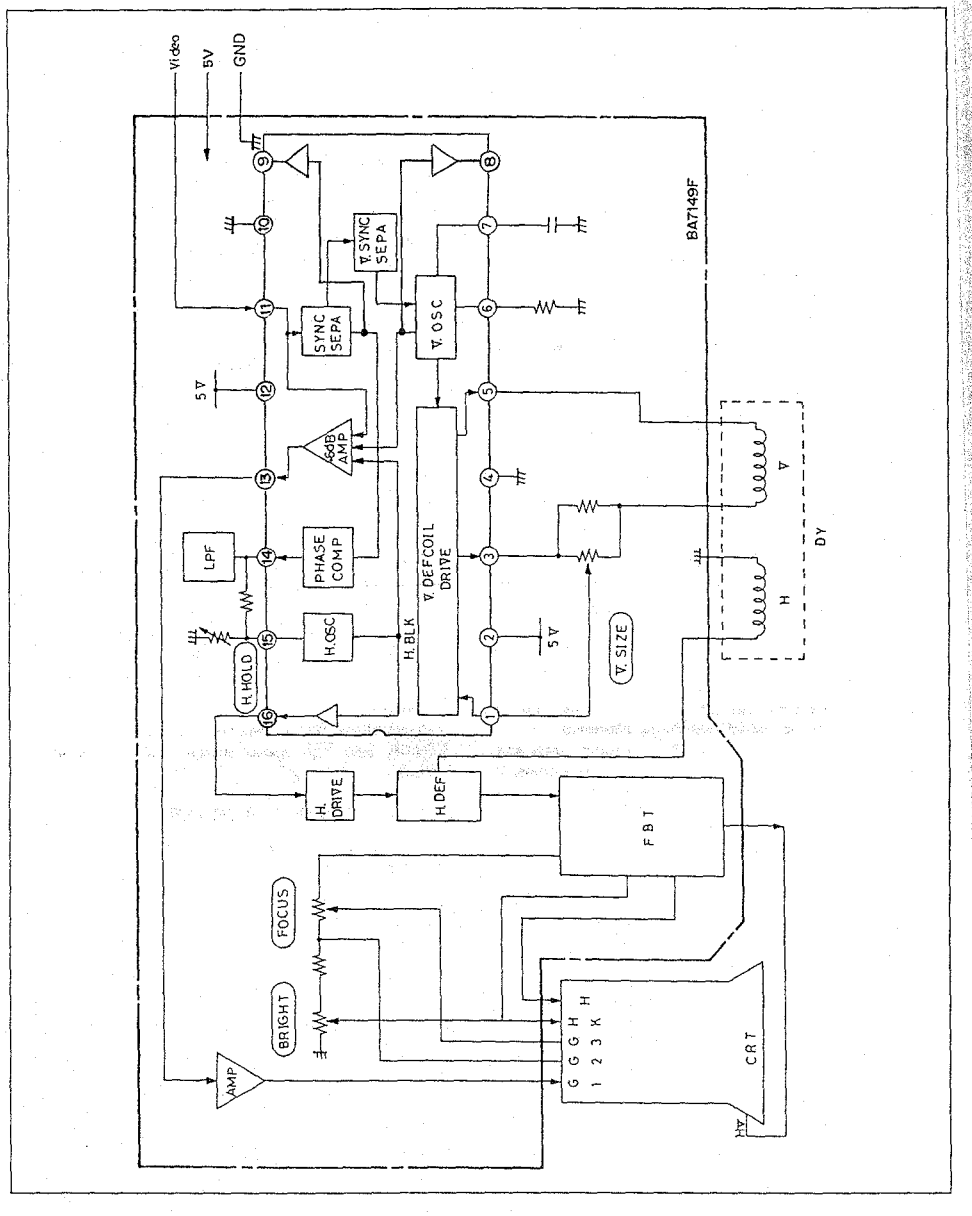
- AF/MF selection switch
- Manual focus switch
- Zoom switch
- NTSC/PAL operation selection switch
- Auto wide reset operation switch
- Camera mode/Video mode selection switch
- Preset mode setting switches (setting switches for sports mode, auto high speed shutter mode, close-up mode, etc.)

2-13. FOCUS MOTOR DRIVER

A stepping motor is used as the focus motor and is driven by the stepping driver IC933. The rotation direction of the focus motor is controlled by Pin ㉔ of the microprocessor IC932 and the speed is controlled by the clock frequency of Pin ㉕ of IC932. When the focus motor stops, because Pin ㉓ of the microprocessor IC932 goes to Low, the REF voltage of the stepping motor driver IC933 drops and current consumption decreases.

3. EVF CIRCUIT OPERATION

3-1. VIEWFINDER BLOCK DIAGRAM



3-2. SYNC SEPARATOR CIRCUIT (SYNC SEPA)

Extracts the sync component from the signal input to Pin ⑪ of the IC1(BA7149F) IC, then sends it through two separate branches to the phase comparator (PHASE COMP) and to the vertical sync separator (V. SYNC SEPA) .

3-3. PHASE COMPARATOR (PHASE COMP)

Compares the voltage obtained by converting the horizontal oscillation waveform into DC at the low-pass filter (LPF) externally attached to Pin ⑭ with the reference voltage during the sync signal period, and controls the horizontal oscillation frequency so that the input signal frequency becomes equal to that of the sync signal. Voltage at Pin ⑭ is affected by changes in input signal frequency (horizontal) .

3-4. HORIZONTAL OSCILLATOR CIRCUIT (H.OSC)

The free-oscillation frequency of this horizontal oscillator depends on the resistor externally attached to Pin ⑮ . A pulse switched by the rising and falling edges of the sawtooth waveform from this oscillator is generated, then supplied through two separate branches to Pin ⑯ as horizontal output and to the video amplifier as horizontal blanking pulse.

3-5. VERTICAL SYNC SEPARATOR CIRCUIT (V. SYNC SEPA)

This circuit separates the sync signal, then extracts the vertical sync component from it.

3-6. VERTICAL OSCILLATOR CIRCUIT (V. OSC)

Free-oscillation frequency of this vertical oscillator depends on the resistor at Pin ⑥ and the capacitor at Pin ⑦.

3-7. VERTICAL DRIVE CIRCUIT (V. DRIVE)

This circuit, provided with a built-in operation amplifier, drives the vertical deflecting coil. An inverted sawtooth waveform voltage is generated from Pins ③ and ⑤. Pin ① is a feedback input used to control the sawtooth wave peak voltage value.

3-8. HORIZONTAL DRIVE & DEFLECTION (H. DRIVE & DEFLECTION)

This circuit applies current amplifying (H.DRIVE) to the horizontal blanking pulse from Pin ⑯, then sends it into the horizontal output transistor. The horizontal deflecting coil (H.DY) and the FBT primary winding parallel inductance are made to resonate with the resonance capacitor, then the first pulse is extracted to generate the FBT input pulse voltage.
At the same time, a sawtooth waveform current synchronized to the H.DY horizontal period is generated from the DC voltage charged by the capacitor inserted serially with H.DY, through the switching operation of the horizontal output transistor.

3-9. HIGH VOLTAGE GENERATING CIRCUIT

The pulse voltage produced by the resonance during the feedback period (see previous paragraph) is boosted by a flyback transformer to generate the CRT grid voltage. CRT anode voltage has a high value of APPROX. 2.2 kV.

4. VIDEO CIRCUIT

4-1. SERIAL CONTROL SIGNAL FOR MODE SELECTION

IC101 (CXA1207AR) (Y signal processing circuit IC) set the mode on the basis of serial control signal data from IC351 (CXP80720) on the same board.

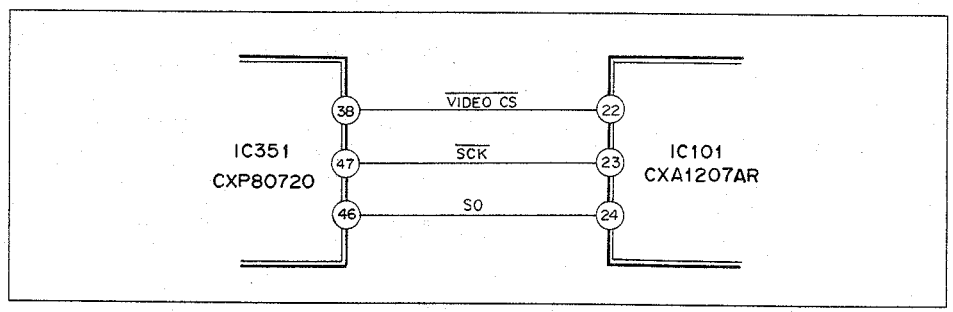


Fig. 4-1. Serial control signal

SCK (clock pulse) and SO (data) are read only when VIDEO CS is low, and the data is latched by the rising edge of VIDEO CS. SO data is detected at the rising edge of SCK.

Operation of IC101 (CXA1207AR) executed by the serial controller is shown in Table 4-1. IC101 (CXA1207AR) mode settings are shown in Table 4-2.

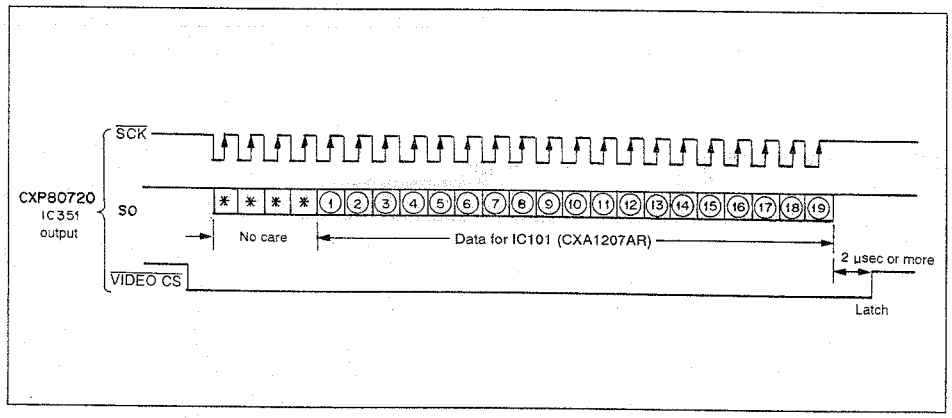


Fig. 4-2. Timing chart

<table>
<tr><th>SIGNAL IN</th><th>HIGH</th><th>LOW</th></tr>
<tr><td>① CORRE OFF</td><td>Y correlation pulse is always LOW.</td><td>Y correlation pulse is output by the Y correlation detection.</td></tr>
<tr><td>② YD</td><td>Performs the YD signal playback when playing back.</td><td>Play back the normal Y signal at playback.</td></tr>
<tr><td>③ NCLP2
④ NCLP1
⑤ NCL2
⑥ NCL1</td><td colspan="2">
<table>
<tr><th>NCL1</th><th>NCL2</th><th>NCLP1</th><th>NCLP2</th><th>1 MHz Freq. Res.</th></tr>
<tr><td>L</td><td>L</td><td rowspan="4">L</td><td rowspan="4">L</td><td>–0.2dB</td></tr>
<tr><td>H</td><td>L</td><td>–3.5dB</td></tr>
<tr><td>L</td><td>H</td><td>–5.7dB</td></tr>
<tr><td>H</td><td>H</td><td>–8.0dB</td></tr>
</table>
<table>
<tr><th>NCL1</th><th>NCL2</th><th>NCLP1</th><th>NCLP2</th><th>1 MHz Freq. Res.</th></tr>
<tr><td rowspan="4">H</td><td rowspan="4">H</td><td>L</td><td>L</td><td>–8.0dB</td></tr>
<tr><td>H</td><td>L</td><td>–10.3dB</td></tr>
<tr><td>L</td><td>H</td><td>–11.8dB</td></tr>
<tr><td>H</td><td>H</td><td>–13.4dB</td></tr>
</table>
There are the level is noise canceler at 1 MHz.
1 MHz/10 kHz frequency characteristics in –30dB input.
</td></tr>
<tr><td>⑦ CFL2
⑧ CFL1</td><td colspan="2">
<table>
<tr><th>CFL2 \ CFL1</th><th>H</th><th>L</th></tr>
<tr><td>H</td><td>–10dB</td><td>–6dB</td></tr>
<tr><td>L</td><td>–1.5dB</td><td>0dB</td></tr>
</table>
These are the level of the Y comb filter.
</td></tr>
<tr><td>⑨ E</td><td>High eight mode</td><td>Normal mode</td></tr>
<tr><td>⑩ CAMERA REC</td><td>Corresponds to CAMERA REC</td><td>Corresponds to LINE REC</td></tr>
<tr><td>⑪ DOC OFF</td><td>Dropout compensation is OFF.</td><td>Dropout compensation is ON.</td></tr>
<tr><td>⑫ EDIT</td><td>Selects EDIT mode.</td><td>Selects NOT EDIT mode</td></tr>
<tr><td>⑬ CCIR443</td><td>fsc=4.43 MHz</td><td>fsc=3.58 MHz</td></tr>
<tr><td>⑭ W CCD</td><td>Used two CCD DLs.</td><td>Used one CCD DL.</td></tr>
<tr><td>⑮ DISCHARGE ON</td><td>Discharges the clamp capacity electric charge of Pins ㉜ and ㉞.</td><td>Does not discharge the clamp capacity electric charge of Pins ㉜ and ㉞.</td></tr>
<tr><td>⑯ AGC ON</td><td>VIDEO AGC ON</td><td>VIDEO AGC OFF</td></tr>
<tr><td>⑰ INSEL</td><td>Selects Pin ㉞ input.</td><td>Selects Pin ㉜ input.</td></tr>
<tr><td>⑱ S</td><td>Separate signal input</td><td>Composite signal input</td></tr>
<tr><td>⑲ PB</td><td>PB</td><td>REC</td></tr>
</table>

Table 4-1. Description of each mode of IC101 (CXA1207AR)

No.	Mode / Data	REC	PB	JOG	No.	Mode / Data	REC	PB	JOG
1	CORRE OFF	H	L	H	11	DOC OFF	L	←	H
2	YD	L	←	←	12	EDIT	L	←	←
3	NCLP2	L	←	←	13	CCIR 443	H	←	←
4	NCLP1	SP:L LP:H	←	←	14	WCCD	L	←	←
5	NCL2	H	←	←	15	DISCHARGE ON	L	←	←
6	NCL1	L	←	←	16	AGC ON	H	L	←
7	CFL2	SP:L LP:H	←	←	17	INSEL	H	L	←
8	CFL1	SP:H LP:L	←	←	18	S	H	L	←
9	E	L	←	←	19	PB	L	H	←
10	CAMERA REC	H	L	←					

Table 4-2. Mode setting of IC101 (CXA1207AR)

4-2. LUMINANCE SIGNAL RECORDING SYSTEM

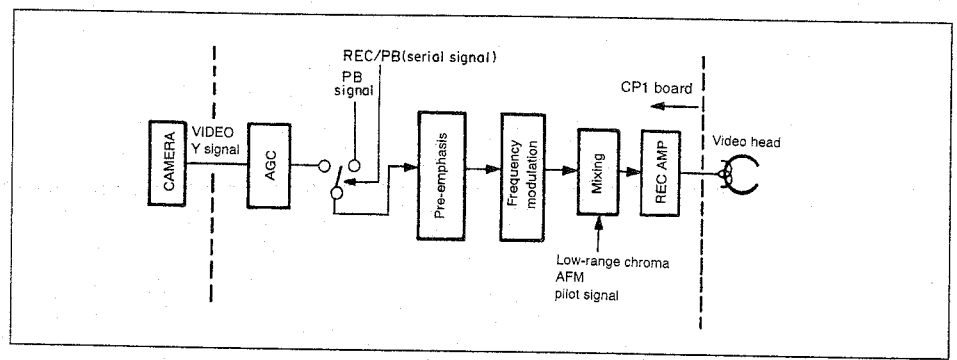


Fig. 4-3. Recording system block diagram

The separated Y (luminance) and C (chroma) signals from the camera block are input to the video block. Both are mixed and sent to the monitor as EE signal.

4-2-1. Input Selector Circuit

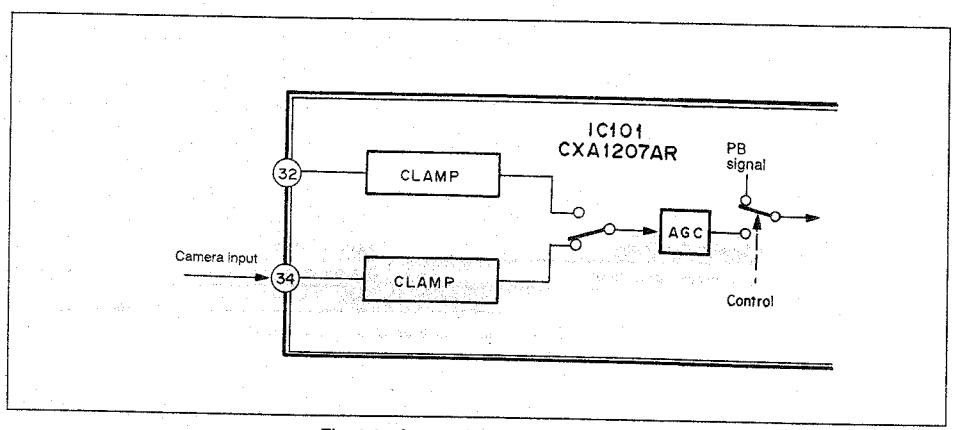


Fig. 4-4. Input selector block diagram

Selection between camera and playback inputs is performed by the serial control signal (SO) from Pin ㉔ of IC101 (CXA1207AR). The serial control signal selects camera (Pin ㉞ of IN2) input, and the playback input (Pin ② of PBIN) is selected in the playback mode (refer to Table 4-3).

INSEL1 / INSEL2	H	L
⑰ INSEL	Camera input (Pin ㉞)	—
⑲ PB	PB	REC

Table 4-3. Serial control signal data

4-2-2. AGC Circuit

This circuit uses the SYNC + PEAK AGC system to maintain input signal level constant. Sync-tip of the video signals input to Pin ㉞ of IC101 (CXA1207AR are clamped, then it is sampled by the AGC pulse and the error signal is feed back to the AGC amplifier. Since the circuit is designed so that peak AGC is applied in proportion to SYNC AGC, only one adjustment control is required.

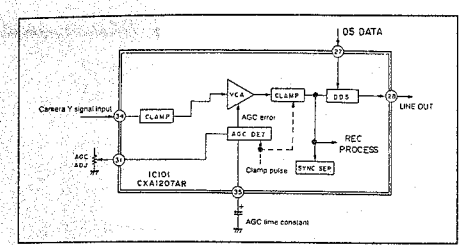


Fig. 4-5. AGC circuit

4-2-3. Y/C Separator Circuit

Since the Y and C signals are separately input from the camera block when camera input, the Y/C separation is not made actually. However in playback they pass through the same line, so the adjustment for the comb filter is necessary.

At this time, from the ADJ. mode, the composite video signal in which the Y and C signals are mixed is input.

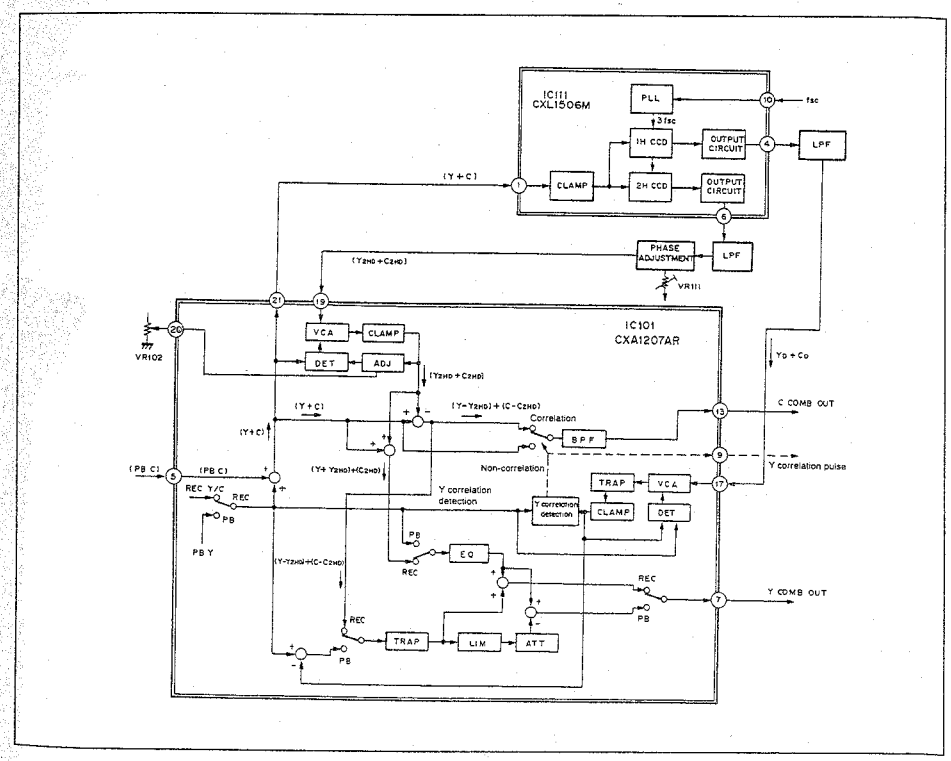


Fig. 4-6. Y/C separator circuit

(1) Y signal separation

The composite video signal is output from Pin ㉑ of CXA1207AR according to the switch shown in Fig. 4-6. Y/C separation circuit line and is input to Pin ① of IC111 (CXL1506M) for CCD delay line. The signal input to the Pin ① is delayed 2H by CCD 2H delay line and is output from Pin ⑥. The signal output from Pin ⑥ passes through the low-pass filter for the clock elimination and the delay time adjustment and is input to Pin ⑲ of IC101 (CXA1207AR) via the phase adjustment circuit.

The 2H delaying signal (Y_{2HD}+C_{2HD}) input from the Pin ⑲ passes through the gain adjustment circuit composed of the VCA, CLAMP, ADJ and DET circuits, becomes (Y+Y_{2HD})+(C+C_{2HD}) ≒ 2Y by adding the original signal (Y+C), and is output to Pin ⑦ before output to Pin ⑦. The section where there is no Y correlation is compensated by adding as only (Y–Y_{2HD}) after eliminating the chroma components of (Y–Y_{2HD})+(C–C_{2HD}) signal with 4.43 MHz TRAP.

Note) C_{2HD} ≒ –C, Y ≒ Y_{2HD}

(2) C signal separation

C signal separation does not pass through the Y/C separation comb filter in order to suppress the color blur in the vertical direction to minimum.

The original signal (Y+C) passes through the switch which is controlled by Y correlation signal, is extracted only the chroma component through BPF, then is output from Pin ⑬.

In PAL system, the switch controlled by Y correlation signal is fixed to the non-correlation side whether there is a correlation or not.

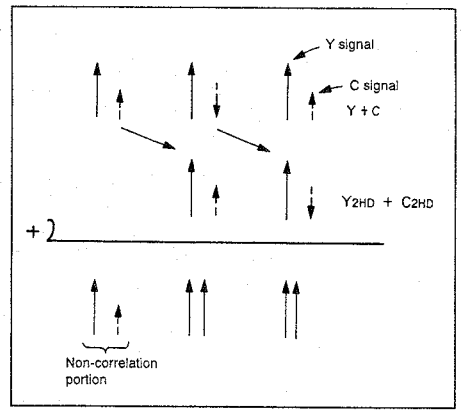


Fig. 4-7. Y signal separation

4-2-4. Pre-emphasis Circuit

(1) Operating principle

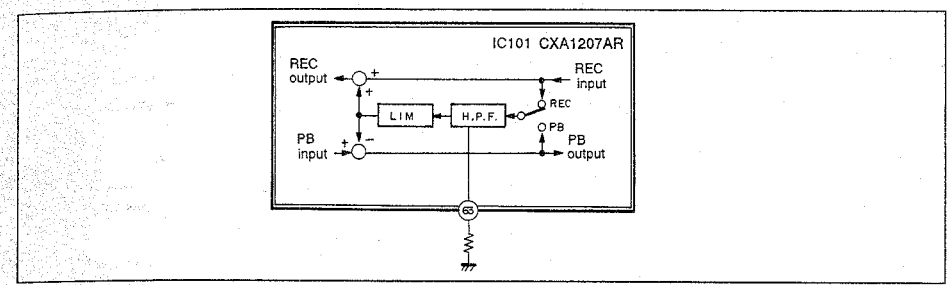


Fig. 4-8. Emphasis/de-emphasis circuit

The transmission function H (S) REC for recording is:

$$H(S)_{REC} = 1 + (1 - \frac{1}{1+SCR})\,G$$

$$= \frac{1+SCR\,(1+G)}{1+SCR}$$

Emphasis time constant T=CR (1+G)

Non-linear emphasis characteristics can be obtained by passing the high-frequency component extracted by the HPF through the limiter.

The transmission function H (S) PB for playback is:

$$H(S)_{PB} = \frac{1+SCR}{1+SCR\,(1+G)} = \frac{1}{H(S)_{REC}}$$

Thus, the inverse of the recording transmission function can be obtained using the same time constant and non-linear circuit.

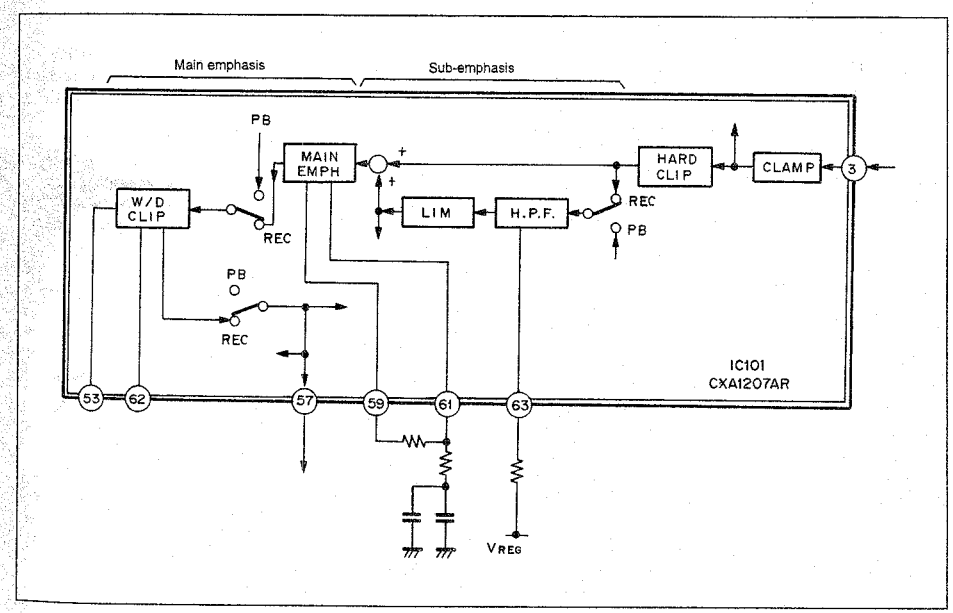


Fig. 4-9. Pre-emphasis circuit

(2) Pre-emphasis circuit

The pre-emphasis circuit is composed of a sub-emphasis circuit and a main emphasis circuit. The sub-emphasis circuit applies non-linear emphasis, and the main emphasis circuit applies linear emphasis and perform WHITE and DARK clipping.

[Hard clip circuit]

The Hard clip circuit operates only during recording when the input level at Pin ③ is too high to prevent overmodulation, etc.

This circuit operates when the clipping level is approx. 575 mVp-p or more (normally 500 mVp-p).

[Sub-emphasis circuit]

The Y signal input to Pin ③ of IC101 (CXA1207AR) is divided into two paths after passing through the clamp circuit and hard clip circuit. One path goes directly into the adder, and the other into the limiter amplifier via the HPF (high-pass filter). The limiter amplifier output is input to the adder and added to the original signal.

- When input level is low
  (–20 dB for the standard 500 mVp-p input, or lower)
  The high-frequency component of the Y signal extracted by the HPF is input directly, without limiting, to the adder. Thus, a high-range-emphasized Y signal can be obtained at the adder output.
- When input level is high
  (–20 dB for the standard 500 mVp-p input, or higher)
  The high-frequency component of the Y signal extracted by HPF is limited and input at a fixed level to the adder. For this reason, the amount of high-range emphasis applied to the Y signal of output of the adder is inversely proportional to the input level.

[Main emphasis circuit]

The Y signal output from the sub-emphasis circuit is input to the main-emphasis circuit. Emphasis is applied by adding the Y signal high-frequency component but, unlike sub-emphasis, linear emphasis is applied without limiting when an abnormal level is reached. Only when there is an overload input such as over 235% white or over 90% black, the limiter will be activated to control the emphasis level (WHITE/DARK clipping).

This is to limit Y-FM signal's frequency deviation within a reasonable range.

The limiter level setting is determined within the IC when Pins ㊸ and ㊷ are open.

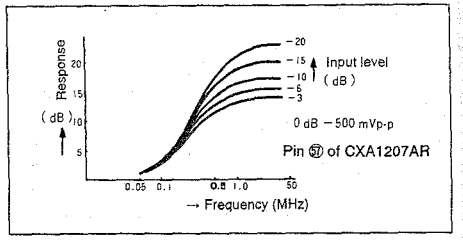


Fig. 4-10. Overall pre-emphasis characteristics

[Half H shift]

In order to eliminate the effects of crosstalk from adjacent tracks (especially horizontal sync signal of adjacent tracks), a 1/2 fH frequency difference is given between CH-A and CH-B.

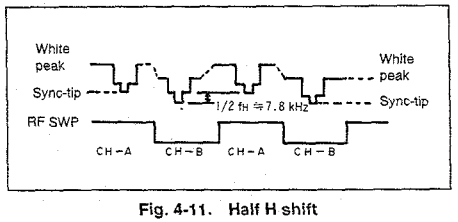


Fig. 4-11. Half H shift

The CH-A signal is shifted by approx. 7.8 kHz, and the beat disturbance caused by crosstalk from adjacent tracks is interleaved against the original demodulated signal in spectral terms.

The sideband energy component of the CH-B track spreads at 1 fH interval. If CH-A track carrier frequency is raised by 1/2 fH, peak and dip sections will coincide, so the crosstalk component can be eliminated by passing the signals through a comb filter during playback (refer to Fig. 4-12).

1/2 fH shift is performed by the frequency modulator.

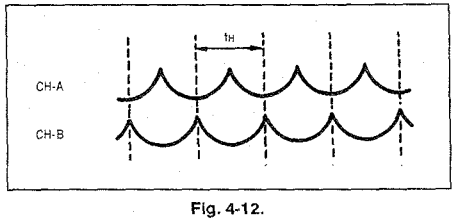


Fig. 4-12.

4-2-5. Frequency Modulator

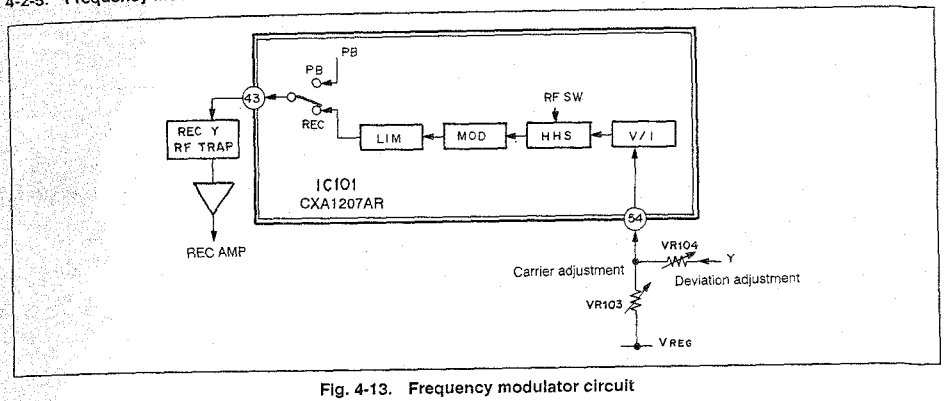


Fig. 4-13. Frequency modulator circuit

The carrier frequency can be set by the carrier adjustment control (VR103) connected to Pin ㊹ of IC101 (CXA1207AR).

It can also be set by varying the Y signal level with the deviation adjustment control (VR104).

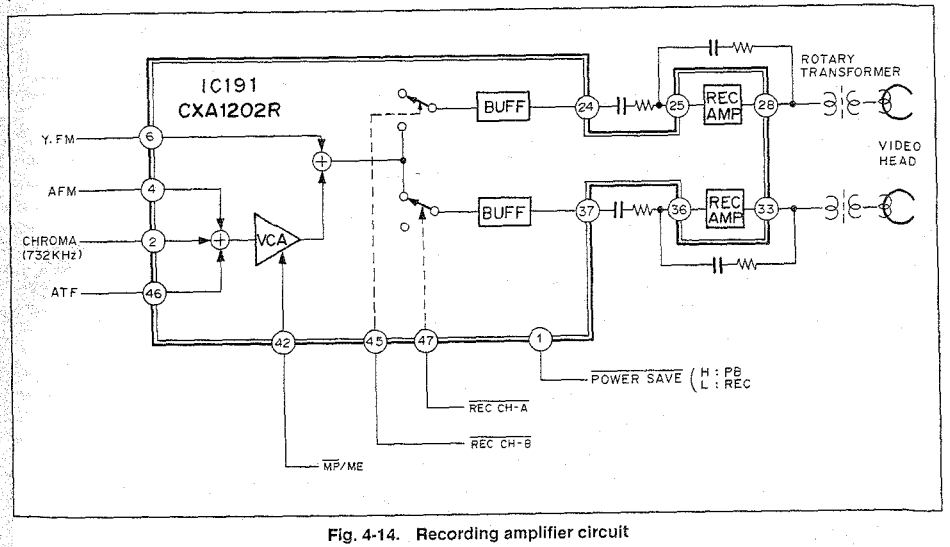


Fig. 4-14. Recording amplifier circuit

4-2-6. Recording Amplifier

Luminance (Y), low-range conversion chroma signal, AFM and ATF signals are input as follows:

Y → Pin ⑥ of CXA1202R (IC191)
C → Pin ② of CXA1202R (IC191)
AFM → Pin ④ of CXA1202R (IC191)
ATF → Pin ㊻ of CXA1202R (IC191)

Chroma (C), AFM and ATF signals are first mixed within IC191 (CXA1202R). The mixed level is adjusted by the DC voltage at Pin ㊷ according to MP/ME tape selection (it is amplified when ME tape is used). The resulting signal is mixed with Y signal input from Pin ⑥, then converted from voltage to current, passes through the recording amplifier and the rotary transformer and is supplied to the video head.

(1) Head Switching and Overlap Processing

In order to reduce power consumption, recording current is only supplied to the side in contact with the tape. This is done by the $\overline{\text{REC CH-A}}$ and $\overline{\text{REC CH-B}}$ signals.

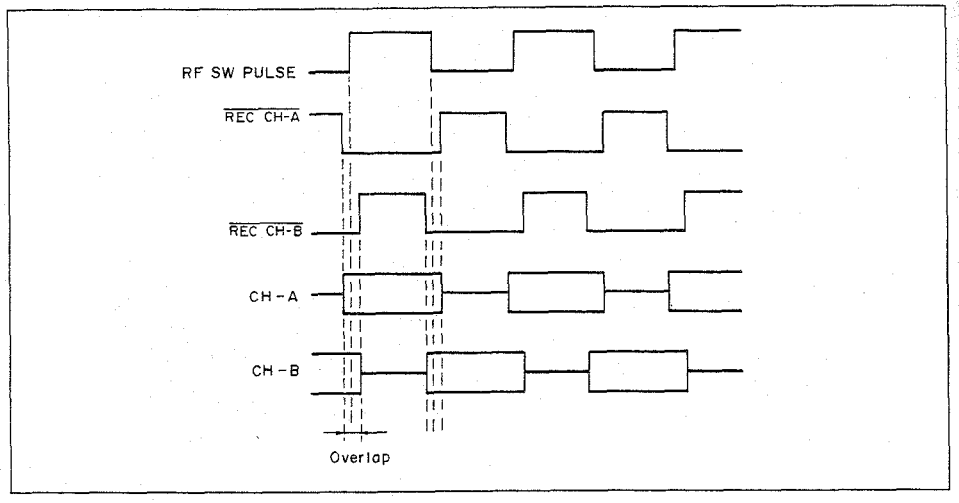


Fig. 4-15. Overlap Processing

(2) Rotary Transformer

This transformer has a 3-CH structure. The winding ratio of the head side to the stator side is 3:5, being stepped up during playback.

Erase head

CH-B (RF SW PULSE − side)

CH-A (RF SW PULSE + side)

(3) Video Head

Video head 2 pieces(track width 27 μm)

Erase head 1 piece(track width 68 μm)

Erase head is not fixed, but works by rotating along the video track.

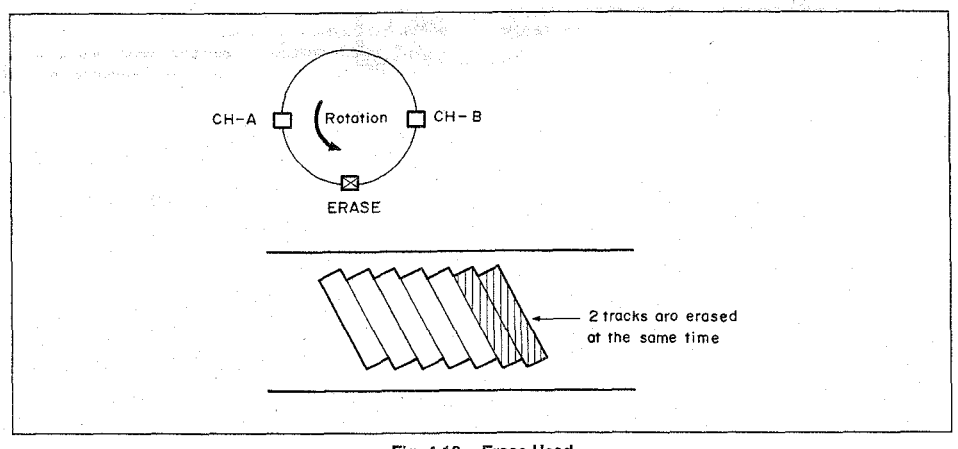


Fig. 4-16. Erase Head

4-3. LUMINANCE SIGNAL PLAYBACK SYSTEM

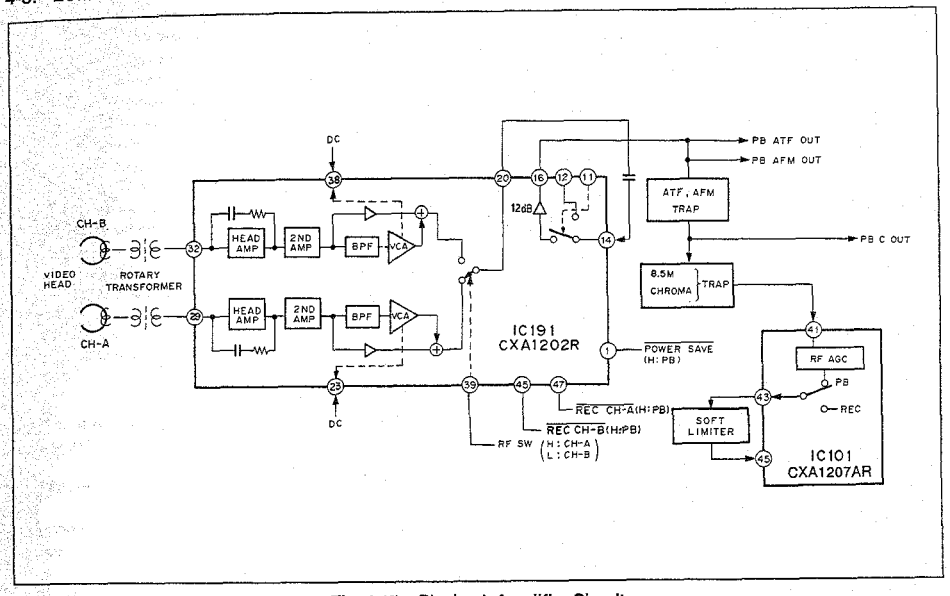


Fig. 4-17. Playback Amplifier Circuit

4-3-1. Playback Amplifier

Explained for CH-A only (same for CH-B)

The playback signal from the head passes through the rotary transformer, then it is fed to the head amplifier through Pin ㉜. Frequency characteristics for playback are flattened by applying feedback damping within the IC in order to limit IC input capacitance and head inductance resonance. The signal for playback frequency correction (middle tune) is tuned to 5.5 to 6 MHz, and correction level is controlled by the voltage at Pin ㉓.

Playback signal switching is controlled by the RF SW pulse input to Pin ㊴. CH-A is selected when the RF SW pulse is "H", and CH-B when it is "L". A continuous signal is obtained at Pin ⑳.

The RF signal output from Pin ⑳ is input to Pin ⑭ and is output from Pin ⑯ via the amplifier of 12 dB inside the IC. After passing through ATF, AFM and C Trap, the signal is fed to Pin ㊶ of IC101 (CXA1207AR) to make the level to certain value by RF AGC. Then, the signal is output from Pin ㊸ of IC101 (CXA1207AR) and the frequency characteristic is compensated according to the input level through the soft limiter circuit, then it is input into Pin ㊺ of IC101(CXA1207AR) and fed to the limiter circuit in the next stage.

(1) Soft limiter

To prevent inversion caused by fluctuation of the head output level, this circuit raises the high-frequency range of the Y-FM signal to compensate the upper side band when the head output level becomes low.

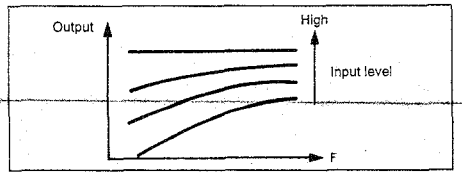


Fig. 4-18. Soft limiter characteristics

4-3-2. Limiter

It eliminates head output fluctuations to maintain a constant level, before the RF signal is input to the frequency demodulator.

When the output level is high, a rectangular wave is produced. When the output level drops, it operates as a linear amplifier, and a normal FM waveform is obtained by emphasizing the high-frequency range. The resulting signal is then turned into a rectangular waveform.

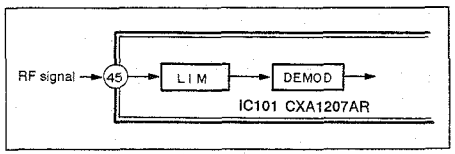


Fig. 4-19. Limiter circuit (inside IC)

4-3-3. Frequency Demodulator

This circuit uses a multivibrator. When the Y-FM signal is added to the non-stable multivibrator, oscillation frequency is locked to the Y-FM signal, generating a constant delay time.

The delay time is constant regardless of the frequency.

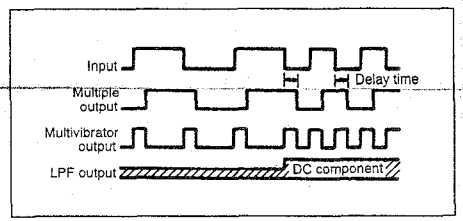


Fig. 4-20. Frequency demodulator

4-3-4. De-emphasis Circuit

The de-emphasis circuit lowers the level of the high-frequency component emphasized at the time of recording to attenuate noise components.

The de-emphasis circuit consists of a main de-emphasis circuit and a sub de-emphasis circuit.

In the main de-emphasis circuit, linear de-emphasis is applied with characteristics reverse to that used for recording. De-emphasis input level is adjusted so that non-linear de-emphasis can be properly performed. This is because non-linear de-emphasis characteristics depend on the input level. The sub de-emphasis circuit performs non-linear de-emphasis using characteristics almost opposite to those at the time of recording.

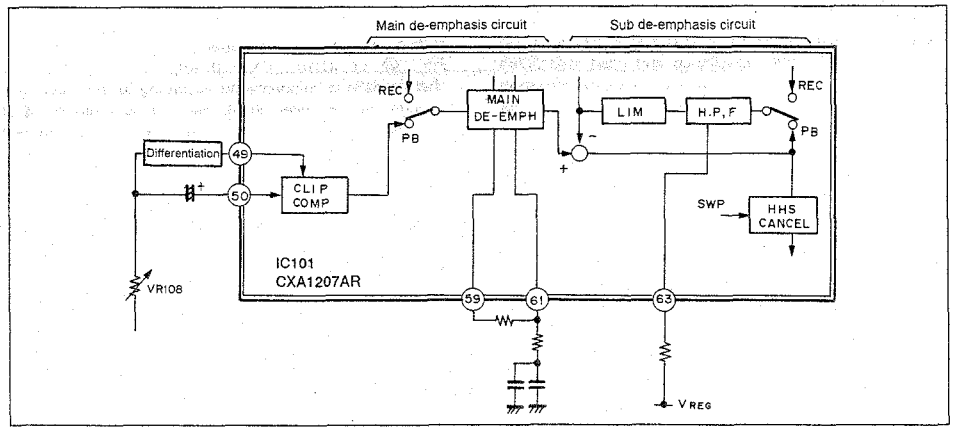


Fig. 4-21. De-emphasis circuit

(1) Clip compensation circuit

This circuit compensates for deterioration of the signal during recording and playback.

(2) Main de-emphasis circuit

Linear de-emphasis characteristics opposite to those used for pre-emphasis are obtained by passing the amplifier output signal through an LPF with the same characteristics used for recording. The capacitor and the resistor located between Pins ⑲ and ⑥① determine main de-emphasis characteristics for playback and main emphasis characteristics for recording.

(3) Sub de-emphasis circuit

Non-linear de-emphasis characteristics nearly opposite to those used for pre-emphasis are obtained by passing the signal output from the subtraction circuit through a limiter and an HPF amplifier with roughly the same characteristics as those used for recording, then feeding it back to the subtraction circuit. As this limiter and HPF are also used for sub-emphasis during recording, exactly opposite characteristics will be obtained if the resistor at Pin ⑥③ has the same value as for recording.

4-3-5. Dropout Compensator

If dropout occurs, the detection pulse actuates the switch and the signal 1H before is output. This switching is carried out either by the RF signal (before demodulation) or the video signal after demodulation.

This IC adopts the latter (the video signal).

Also, because this DOC incorporates AGC in the circuit construction, it becomes the free adjustment.

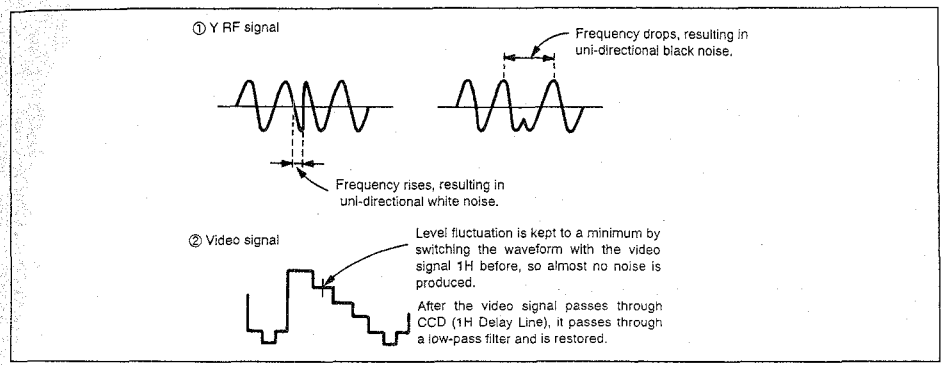

① Y RF signal
Frequency drops, resulting in uni-directional black noise.
Frequency rises, resulting in uni-directional white noise.
② Video signal
Level fluctuation is kept to a minimum by switching the waveform with the video signal 1H before, so almost no noise is produced.
After the video signal passes through CCD (1H Delay Line), it passes through a low-pass filter and is restored.

Fig. 4-22. Dropout compensator

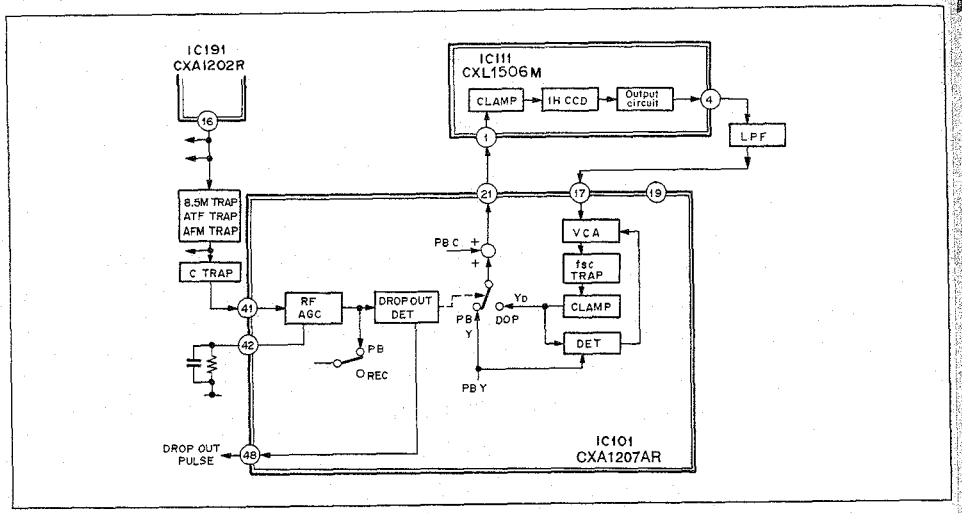


Fig. 4-23. Dropout compensation circuit

After trapping the ATF, AFM and C (chroma) components, the playback Y RF signal is input to Pin ㊶ of IC101 (CXA1207AR) and the level difference between the heads is eliminated at the RF AGC circuit, after which the signal is input to the dropout detector circuit. Here, envelope detection is performed to detect the dropout of playback Y RF signal. A shallow detection will be enough for information with little noise, but a signal such as shown in Fig. 4-24 will produce fluttering. For this reason, the detection circuit is provided with hysteresis characteristics. In IC101 (CXA1207AR), the level difference between the playback Y signal and 1H DL (YD) signal is detected by DET (detector), and voltage controlled amplifier (VCA) gain is adjusted to equal its level to the Y signal. This eliminates any luminance difference between dropout-compensated sections and other sections than dropout of the Y signal.

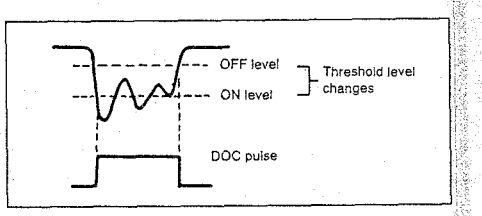


Fig. 4-24. Hysteresis characteristics

4-3-6. Y Comb Filter (Crosstalk Canceler)

Since there is a 1/2 fH offset between CH-A and CH-B tracks playback Y signals, the main signal is interleaved with the crosstalk from adjacent tracks.

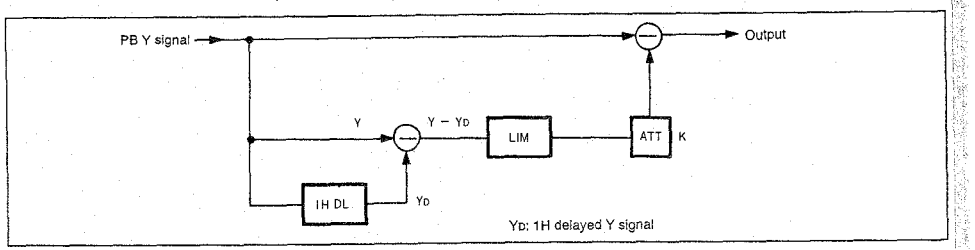


Fig. 4-25. Comb filter

When there is horizontal correlation, Y–YD is small enough to pass through the limiter. When there is no horizontal correlation, however, Y–YD is large and it can hardly pass through the limiter, so the input signal is output unchanged.

For example, if K=1/2, output becomes Y–K (Y–YD)=Y–1/2 (Y–YD)=1/2 (Y+YD), and the effect of the comb filter depends on the degree of correlation. This is called a dynamic comb filter.

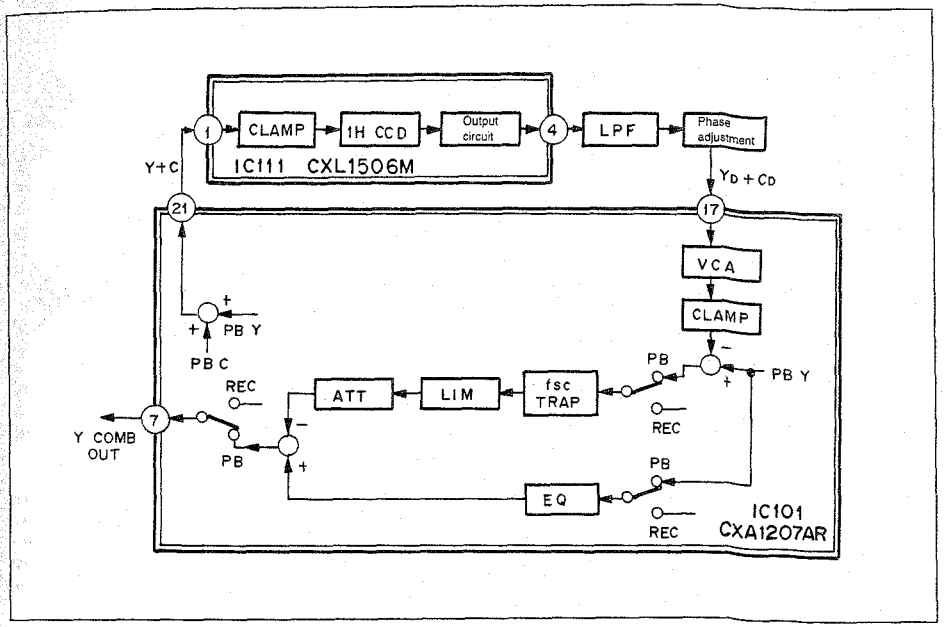


Fig. 4-26. Dynamic comb filter circuit

The playback Y+C signal is input to Pin ① of IC111 (CXL1506M) and the YD+CD signal delayed by 1H CCD is output from Pin ④. The YD+CD signal is input to Pin ⑰ of IC101 (CXA1207AR). The level of the YD+CD signal is matched with the Y signal by the AGC circuit and then subtracted from the Y signal by a subtraction circuit, resulting in the Y–YD–CD signal. Furthermore, the chroma component is removed by an fsc trap to produce a Y–YD signal. The Y–YD signal obtained in this way and the Y signal in IC101 (CXA1207AR) form a dynamic comb filter to cancel CROSSTALK.

4-3-7. Noise Canceler Circuit

(1) Principles of noise cancel

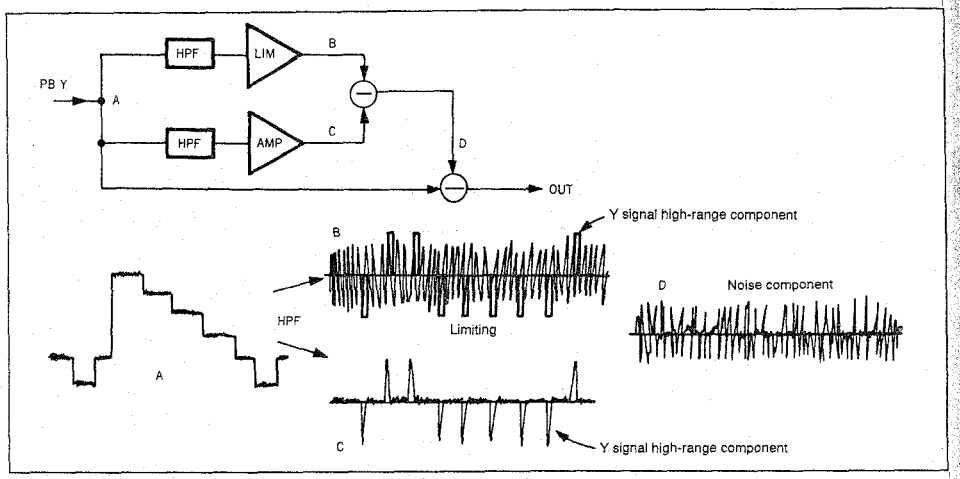


Fig. 4-27. Noise cancel

Since the playback Y signal (PB Y) noise component is almost completely in the high-frequency range, the high-range component is extracted with an HPF. Noise can be thought of as a cluster of small-amplitude signals. It is present particularly in the high-frequency range of the Y signal. There is a high-range component also in the Y signal itself, whose amplitude is considerably larger than that of the noise component. Therefore, the extracted high-range component is limited, the Y signal high-range component is subtracted from the resulting signal and the noise component is extracted. This prevents Y signal high-range component dropouts. After this, the noise component is removed from the original Y signal.

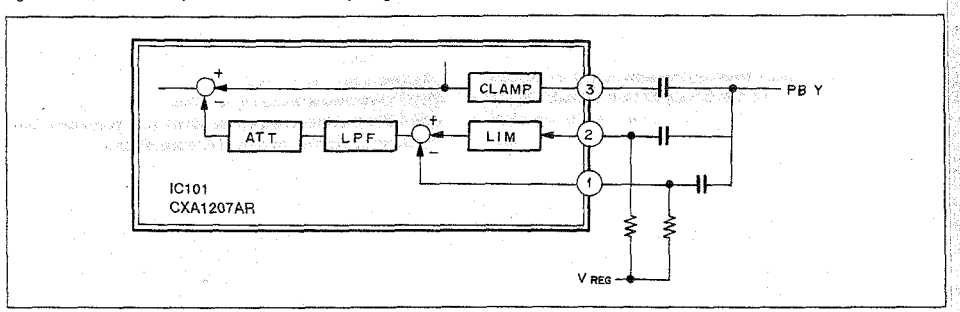


Fig. 4-28. Noise cancel circuit

The playback Y signal is input to Pin ③ of IC101 (CXA1207AR). The high-range component of this signal is extracted by the high-pass filter consisting of capacitor and resistor and then fed to Pin ① and Pin ②. The Pin ② input is fed to the subtraction circuit via the LIM circuit, and then subtracted from the Pin ① input to compensate the Y signal high-range component for noise component extraction.

After that it passes through the LPF, its level is set at the attenuator circuit and it is subtracted from the original Y signal to generate the Y signal with its noise component subtracted.

Although the noise cancellation amount is set by the serial control signal, the characteristics is determined by the capacitor and the resister of Pin ① and Pin ②.

4-3-8. Character Insertion Circuit and VD Insertion Circuit

Insert the date in EE mode, with the analog SW IC141 (NJM2235M).

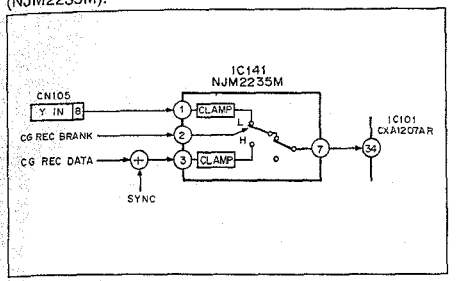


Fig. 4-29.

VD and HD insertion circuit

When playback, if Pin ㉛ of IC101 (CXA1207AR) is set to "H" at the timing of VD and HD, the potential is changed into sink chip one in the DDS circuit at this period.

Accordingly VD and HD are inserted into regenerative signals.

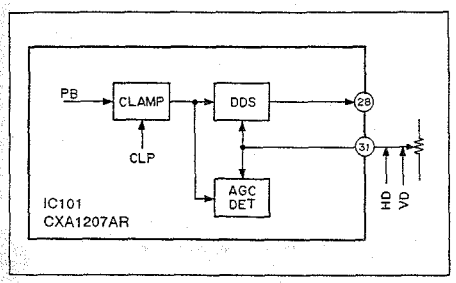


Fig. 4-30. VD and HD insertion circuit

Character insertion circuit (1)

In CXA1207AR the character signal is inserted to the DDS circuit inside the IC by applying the OS DISP BLANK pulse into Pin ㉙ and the OS DISP DATA pulse into Pin ㉗ in the ON SCREEN mode. (Fig. 4-31)

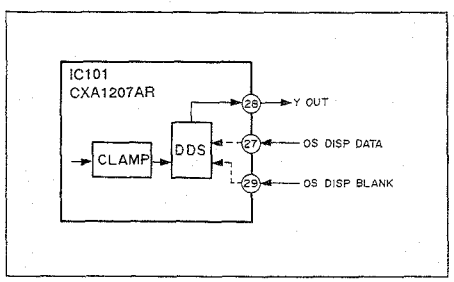


Fig. 4-31. Character insertion circuit

4-3-9. Output Circuit

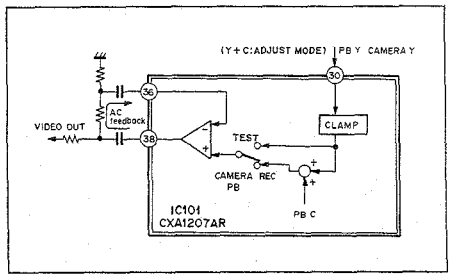


Fig. 4-32. Video output circuit

This circuit sends the EE output or the playback signal to the monitor TV.

The video output circuit consists of an operational amplifier. AC feedback loop is applied externally for gain control.

4-4. CHROMA SIGNAL RECORDING SYSTEM

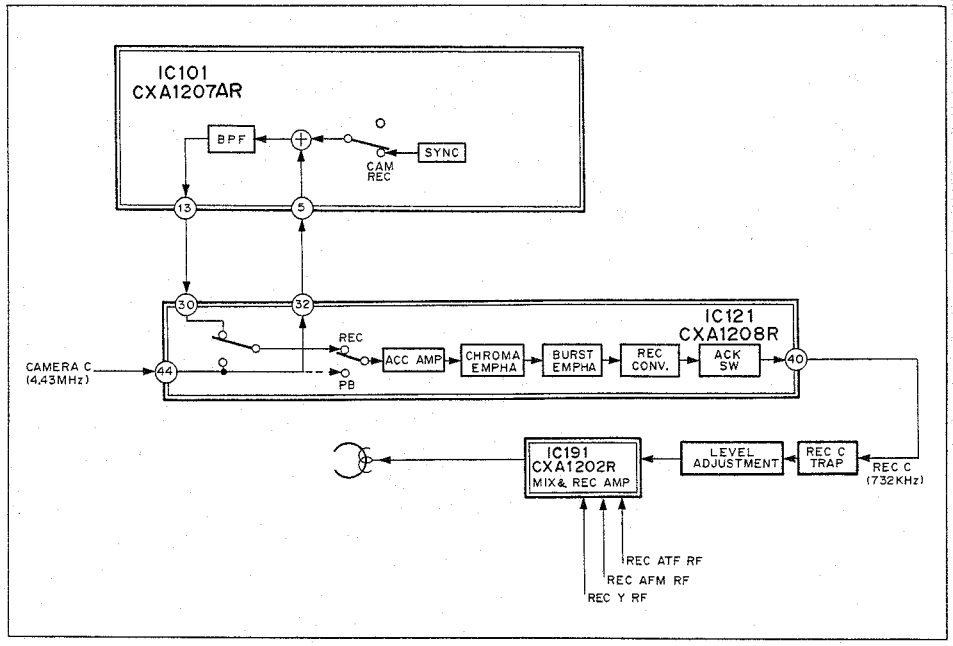


Fig. 4-33. Chroma signal recording system block diagram

4-4-1. ACC Circuit

4.43 MHz chroma signal level is adjusted by controlling ACC amplifier gain so as to keep burst level constant.

Note 1) The recording system does not perform switching of the time constant for each field by RF SW pulse.

Note 2) The capacitor for holding is built into IC121 (CXA1208R).

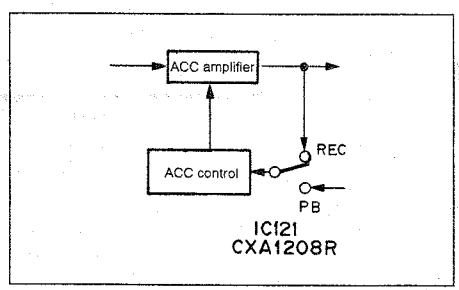


Fig. 4-34. ACC circuit

4-4-2. Chroma Emphasis Circuit

S/N ratio is improved by emphasizing the chroma signal sidebands range during recording, then de-emphasizing it during playback. The chroma signal sidebands range is susceptible to noise influence due to the low level of its spectrum component.

In this circuit, when the chroma signal level is high, emphasis is not applied. The amount of emphasis increases as level decreases. The amount of emphasis is small near the sub-carrier center, and larger as one moves away from the center.

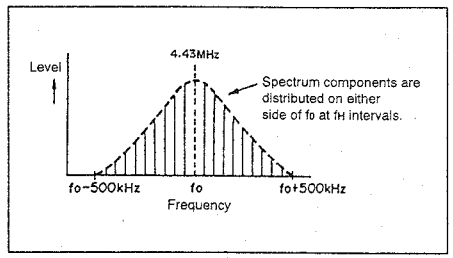


Fig. 4-35. Chroma signal spectrum

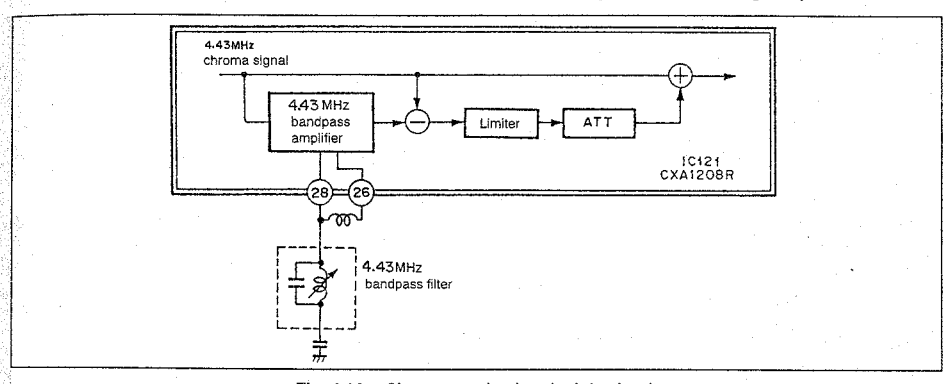


Fig. 4-36. Chroma emphasis principle circuit

The sidebands components are removed from the original 4.43 MHz chroma signal from the burst emphasis circuit by the 4.43 MHz bandpass amplifier. The sidebands components are extracted by subtracting this signal from the original signal with a subtractor, then they are added to the input signal after passing through the limiter and attenuator circuits.

The limiter output level is kept constant by the limiter regardless of the input chroma signal level. Thus, the amount of emphasis is non-linear.

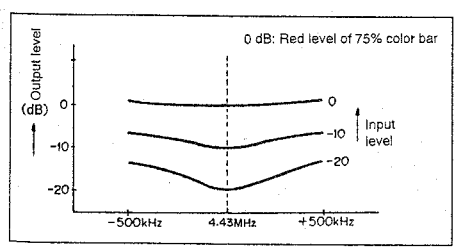


Fig. 4-37. Chroma emphasis characteristics circuit

4-4-3. Burst Emphasis Circuit

Burst signal noise is canceled, thus improving the S/N ratio of the color signal, by boosting the burst signal level when recording and returning it to the original level during playback.

The burst emphasis circuit increases amplification gain only during the burst period by the burst flag.

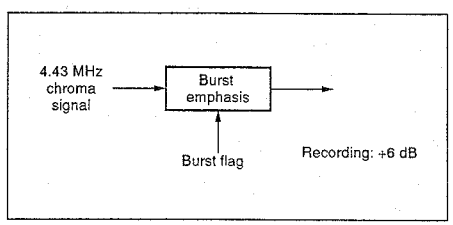


Fig. 4-38. Burst emphasis

4-4-4. Frequency Conversion Circuit

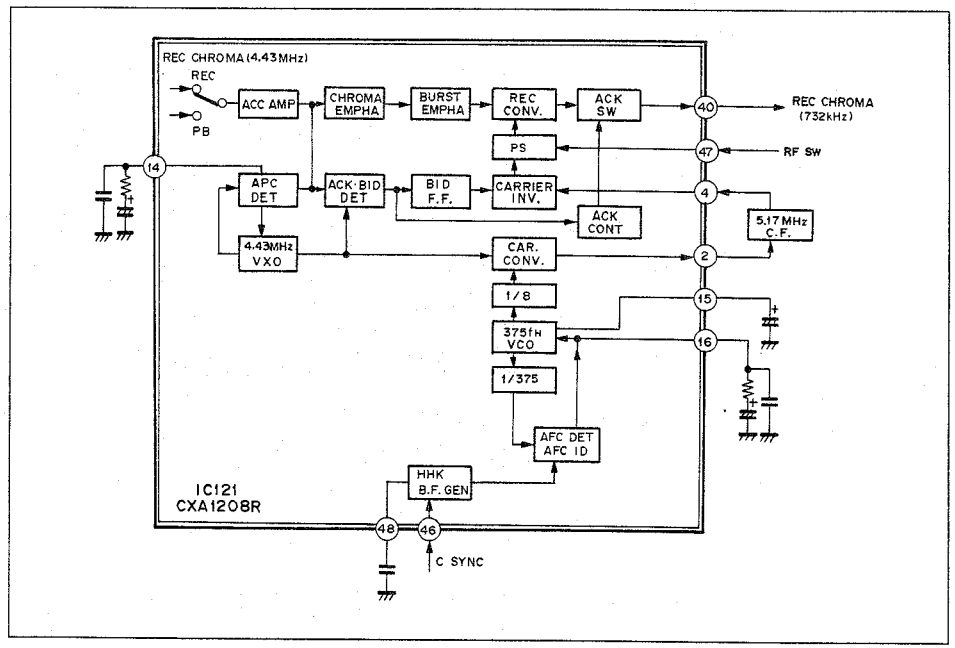


Fig. 4-39. Frequency conversion block diagram

The frequency conversion system of the recording system is composed of a frequency conversion circuit, an AFC circuit and an APC circuit. It changes frequency of the chroma signal from 4.43 MHz to 732 kHz.

Frequency conversion system

- Frequency conversion circuit
  - Carrier converter
    Creates a 5.17 MHz signal from the APC circuit 4.43 MHz signal and the AFC circuit 732 kHz signal.
  - PS circuit
    For CH-B field only, shift the phase of the 5.17 MHz signal shifted 90° by every 1H.
  - Chroma converter
    Changes frequency of the chroma signal from 4.43 MHz to 732 kHz.
- AFC circuit ..... Creates a 732 kHz (47–1/8) • fH signal phase-locked to H. SYNC, which has been separated from the input video signal.
- APC circuit ..... Creates a 4.43 MHz signal phase-locked to the burst signal which has been separated from the input video signal.

(1) Chroma converter

Frequency of the chroma signal is changed from 4.43 MHz (fsc) to 732 kHz ((47–1/8) fH) by the 5.17 MHz (fsc+(47–1/8) fH) frequency-conversion carrier. As spurious components are generated at the same time, these are removed by the REC chroma trap.

This trap is composed of a 732 kHz ± 500 kHz BPF and a 1.5 MHz trap. The former deletes the Y-FM and AFT signals which exist in the chroma-band. The latter deletes the AFM signals from the chroma-band.

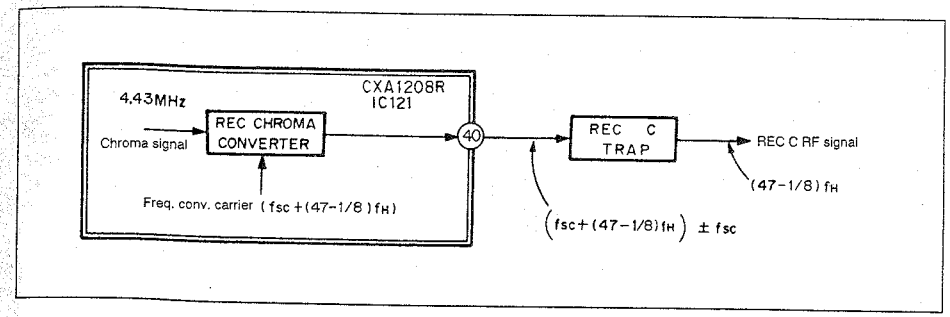


Fig. 4-40. Chroma converter

(2) Carrier converter

The carrier for frequency conversion is created from the (47–1/8) fH (approx. 732 kHz) signal created by dividing the 375fH VCO by 1/8 within the IC121 (CXA1208R) and the 4.43 MHz signal. Any spurious components generated at the same time are removed by a ceramic filter.

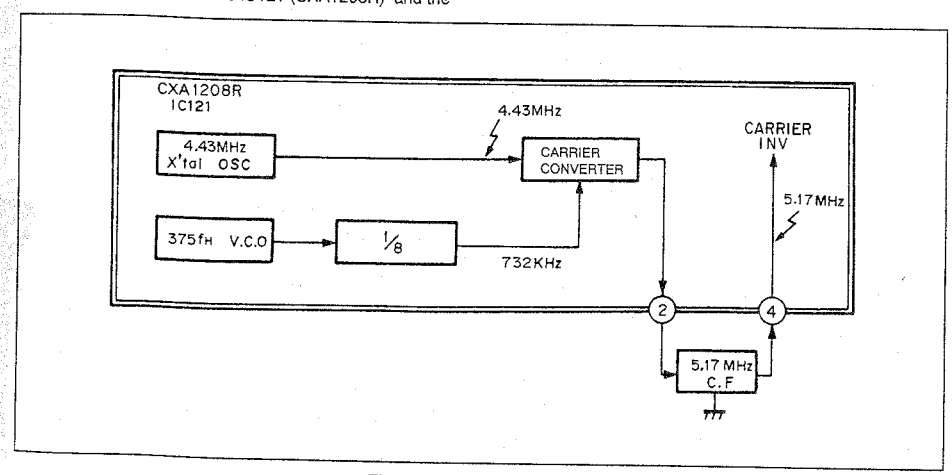


Fig. 4-41. Carrier converter

(3) PS circuit

The phase of the carrier for frequency conversion is shifted 90 ° by every 1H only when the CH-B video head is in use (when RF SW pulse is "L").

This operation invert only the phase of the CH-B field of the low-range conversion chroma signal shifted 90 ° by every 1H. Through this signal processing, phase of the crosstalk component in the playback chroma signal is inverted in relation to the original signal every 2H, which allows the comb filter to remove it. This method of signal processing is called PS (Phase Shift) system.

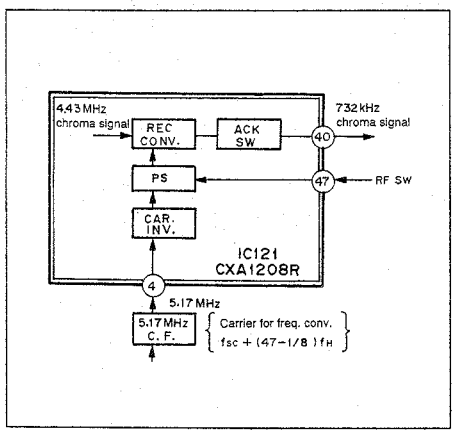


Fig. 4-42. PS circuit

(4) APC circuit

During recording, the APC circuit produces a 4.43 MHz signal phase-locked to the burst signal in the chroma signal.

The chroma signal output from the ACC amplifier and the signal from the 4.43 MHz VXO (Variable X'tal Oscillator) are input to the APC detection circuit. These two signals are detected in the APC detection circuit only during burst periods by the burst flag signal, and the APC error voltage is obtained by integrating the detected wave by the APC LPF externally connected to Pin ⑭ of IC121 (CXA1208R).

By feeding back this APC error voltage to the 4.43 MHz VXO, the oscillation frequency output from the 4.43 MHz VXO is phase-locked to the color burst signal within the chroma signal output by the ACC amplifier.

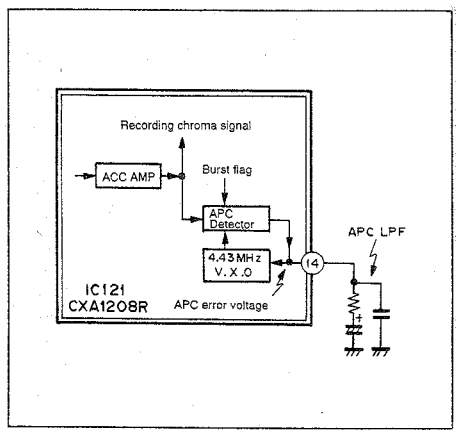


Fig. 4-43. APC circuit

(5) AFC circuit

During recording, the AFC circuit produces a (47–1/8) • fH (approx. 732 kHz) signal which is phase-locked to the H. SYNC signal of the input video signal.

The output of the 375 • fH VCO is converted to frequency of fH by the 1/375 frequency divider, then input to the AFC detection circuit and the AFC ID detection circuit.

The AFC error signal is obtained by phase comparison between the 1/375 frequency divider output and either of the above input reference H in the AFC detection circuit, then the 375 • fH VCO is phase-locked. The 375 • fH VCO output phase-locked to H. SYNC by this AFC loop is divided to 1/8, then input to the carrier converter.

The AFC ID circuit does not operate while AFC is phase-locked. It only works when the phase is unlocked.

[1/375 frequency divider]

This frequency divider divides 375 • fH VCO output in the following manner to create an fH-interval signal. When used for PAL system, this divider can be set to 1/375 by switching the voltage at Pin ㊶ of IC121 (CXA1208R). Also, the VCO circuit can be set to 375 • fH VCO for the PAL system, by switching the voltage at Pin ㊶.

Pin ㊶	H	L
Mode	PAL	NTSC

[AFC detection]

The phase of the rising edge of the AFC DET input reference H is compared to the 1/375 divider output. The AFC error signal is output according to the phase difference to control the 375 • fH VCO through the LPF connected externally to Pin ⑯ of CXA1208R.

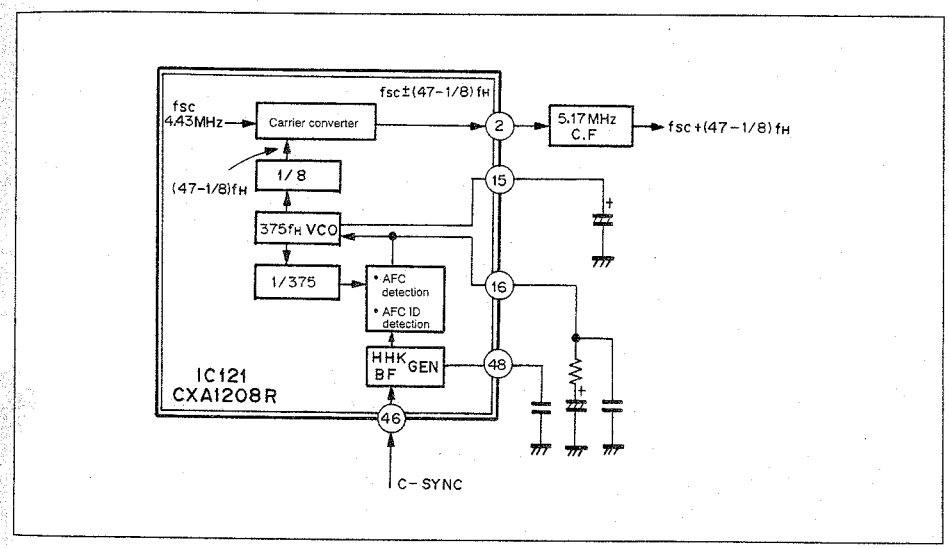


Fig. 4-44. AFC circuit

[AFC ID detection]

AFC ID operates when the rising edge of the 1/375 divider output is shifted by the time determined in IC121 (CXA1208R) from the rising edge of the input reference H to control the 375 • fH VCO oscillation frequency with AFC.

[Half-H killer circuit]

The H. SYNC signal is used as a comparison signal for signal processing such as AFC, AFC ID (for recording) and APC ID (for playback), etc.

This H. SYNC signal is created from the composite SYNC separated from the input video signal. As the composite SYNC signal contains a 1/2H equalizing pulse in the vertical sync signal section, this must be removed.

4-5. CHROMA SIGNAL PLAYBACK SYSTEM

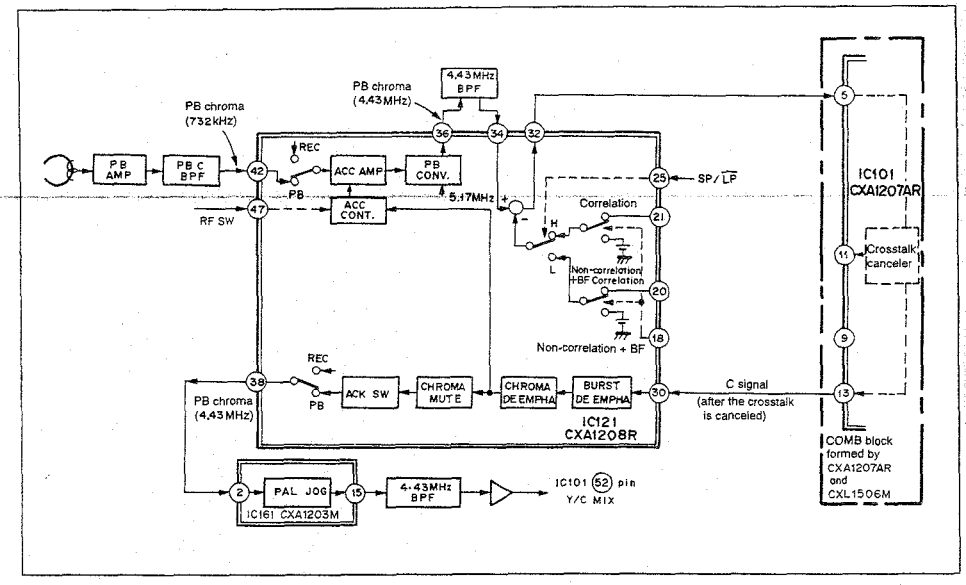


Fig. 4-45. Chroma signal playback system block diagram

4-5-1. Playback Chroma BPF

The Y-FM, AFM and ATF signals are removed from the playback RF signal, thus extracting the playback chroma signal.

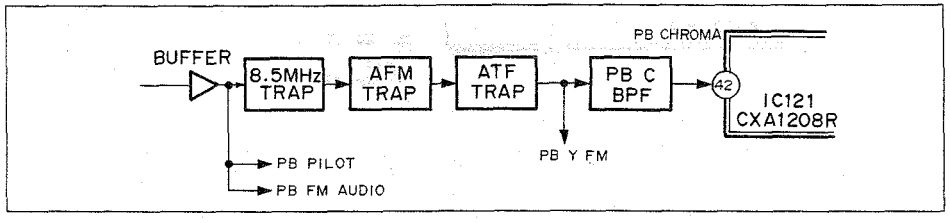


Fig. 4-46. Playback chroma BPF

4-5-2. ACC Circuit

The ACC circuit has the following two functions during playback:

1. Elimination of level fluctuations of the playback chroma signal.
2. Elimination of playback chroma signal level differences between channels caused by video head sensitivity differences.

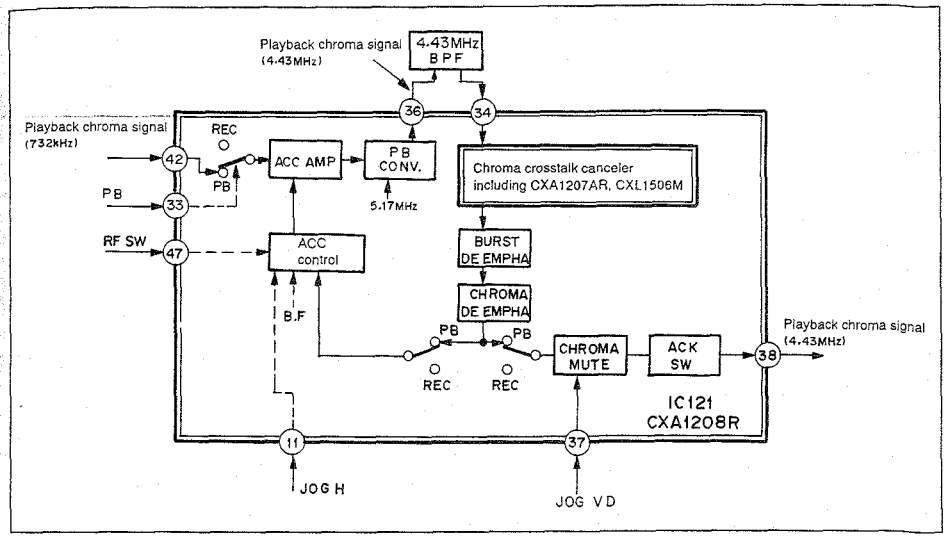


Fig. 4-47. ACC circuit

After playback chroma processing, the playback chroma signal (4.43 MHz) is input to the ACC control circuit. This is to prevent faulty operation of the ACC due to crosstalk and noise components. The ACC control circuit controls the ACC amplifier by detecting the burst signal section of the input playback chroma signal (4.43 MHz) in order to keep the burst signal level of the playback chroma signal (4.43 MHz) constant.

In addition, compensation for video head sensitivity differences is performed by switching over the smoothing capacitor by means of the RF SW.

Note: The ACC smoothing capacitor is built into IC121 (CXA1208R).

[High-speed ACC circuit]

Chroma signal levels make large fluctuations in short intervals during variable speed playback (during picture search, for example, there are three or four large level fluctuations per field).

Consequently, level changes cannot be followed with an ACC loop gain equal to that of the ordinary playback mode. This is solved by using the JOG H signal input to Pin ⑪ of IC121 (CXA1208R) during variable speed playback to switch among loop gain for the ACC circuit.

4-5-3. Frequency Conversion Circuit

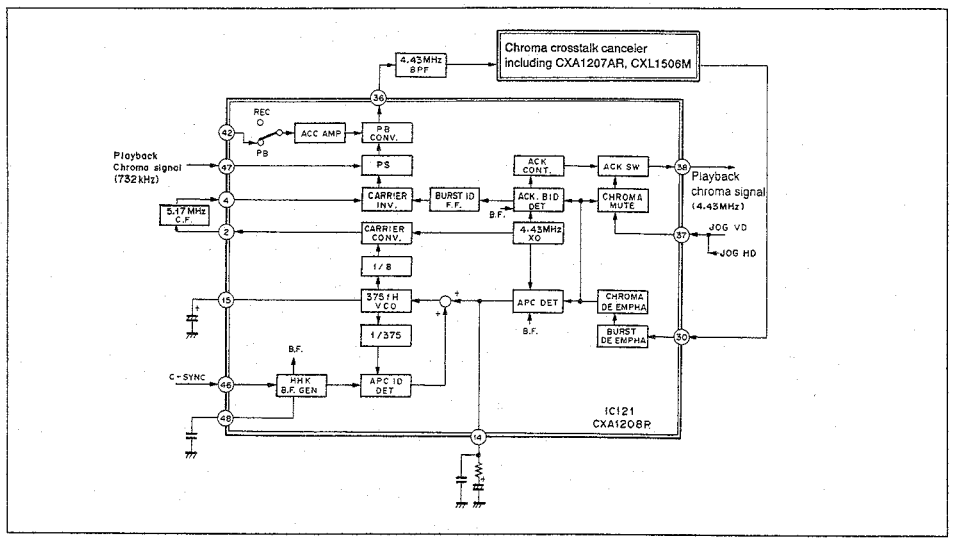


Fig. 4-48. Frequency conversion circuit

During playback, the 4.43 MHz crystal oscillator operates as a fixed oscillator, generating a reference pulse. The jitter component of the playback chroma signal is removed by the APC circuit, and the AFC circuit does not operate. The APC circuit operates so that the burst signal of the playback chroma signal converted to 4.43 MHz is phase-locked to the reference oscillator. The APC ID circuit does not operate while the playback chroma signal is phase-locked by the APC, but starts operation only when there is a shift large enough to unlock the phase.

(1) APC circuit

The 4.43 MHz chroma signal from the chroma converter and the signal from the 4.43 MHz reference oscillator are input to the APC detection circuit.

The phases of the two signals are compared with each other only during the burst period by the burst flag, and the resulting phase difference is applied to the 375 • fH VCO as the APC error. After being divided by 8, the 375 • fH VCO output is used to produce the frequency conversion carrier with the reference oscillator output. This signal converts frequency of the playback chroma signal from 732 kHz to 4.43 MHz. At this APC loop, the burst signal of the 4.43 MHz chroma signal is phase-locked to the reference oscillator output signal, canceling jitter. The reason why the APC error is input into the 375 • fH VCO instead of the reference oscillator is because the frequency variation range of the VCO is wider, producing a larger APC loop gain and thus a wider jitter allowance range as well as a faster response rate.

(2) APC ID circuit

The APC ID circuit is necessary because of the following difficulties encountered when the APC is used alone.

1. There are occasions when color disappears due to improper compensation in case a large frequency error occurs during variable speed playback.
2. Mis-locking can occur in the following cases when a VCO with wide variable frequency is used:

1) APC mis-locking can occur at fsc ± n • fH because of being controlled by sampling every 1H by the burst signal.
2) If there is a crosstalk component in the chroma signal, APC will be phase-locked to this component, and therefore mis-locking will occur at fsc ± 1/2 (2n ± 1) fH.
3) fsc ± 1/2 fH is a quasi-stable point of APC, and therefore mis-locking occurs.

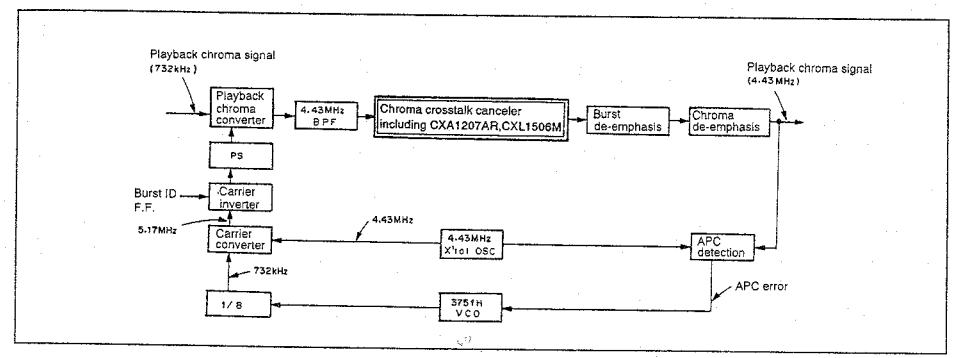


Fig. 4-49. APC circuit

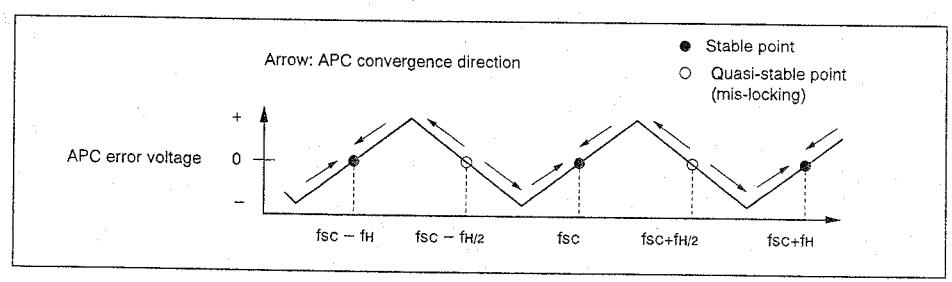


Fig. 4-50. APC ID characteristics

4-5-4. Chroma Comb Filter

As shown in Fig. 4-53, the chroma comb filter for playback consists of a part of IC121 (CXA1208R), IC101 (CXA1207AR) and the CMOS-CCD 2H delay line IC111 (CXL1506M).

This filter is used for chroma signal playback processing and for removing the chroma signal crosstalk component from the adjacent track.

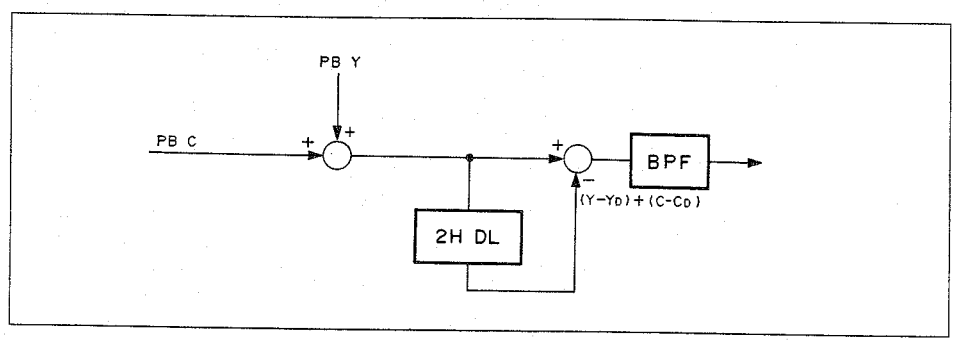


Fig. 4-51. Comb filter

Since the crosstalk in the adjacent track is recorded in PS system, it is shifted at 90 ° against the original signal. Making use of this, subtract the original signal and CCD 2H delayed signal, thus the crosstalk component is canceled and the original chroma signal can be processed in double signal level. (See Fig. 4-52.)

After that, the playback chroma signal which has canceled the crosstalk can be obtained by passing through the BPF to eliminate the PB Y component (Y–YD).

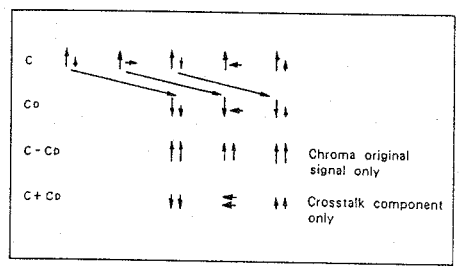


Fig. 4-52. Comb filter

Signal flow is then explained following that in Fig. 4-53.

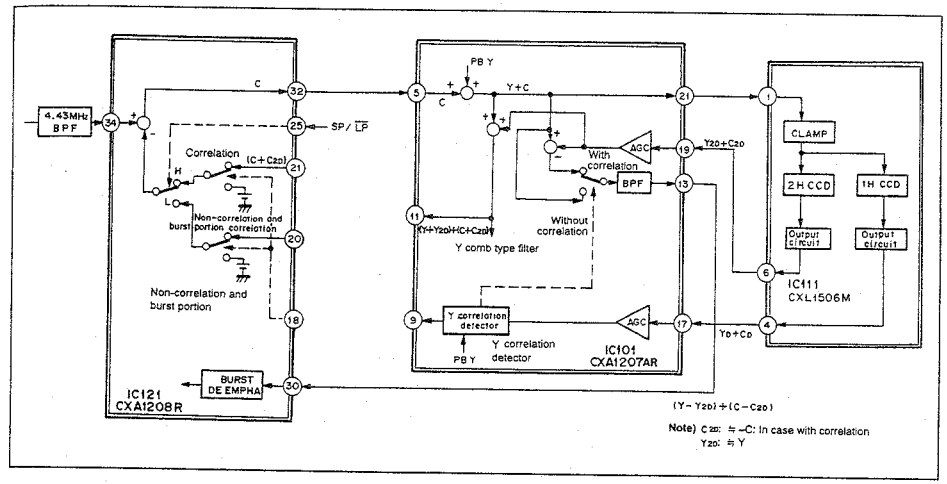


Fig. 4-53. Chroma comb type filter

[Non-feedback type comb filter]

The playback chroma signal that includes crosstalk components, is passed through a band-pass filter, sent to Pin ㉜ of IC121 (CXA1208R) where the signal is passed through the subtractor and fed to its Pin ㉜ . (It is not performed subtraction, as signal is not input from Pin ㉑ and ⑳ of IC121.)

The output signal of Pin ㉜ is then sent to Pin ⑤ of IC101 (CXA1207AR) where the playback chroma signal is added to the playback Y signal by the adder to produce the (Y+C) signal that output from Pin ㉑ . The (Y+C) signal is then input to Pin ① of IC111 that is a CCD delay line type CXL1506M where the signal is delayed for 2 horizontal period to produce the 2H delayed ($Y_{2D}+C_{2D}$) signal which is output through Pin ⑥ of IC111. And the 1H delayed (Y_D+C_D) signal is sent to Pin ⑰ of IC101 (CXA1207AR) where an internal AGC circuit controls the signal level for a constant output amplitude, and the AGC output is sent to a " Y correlation detection" circuit to be used for judgment whether the previous Y signal and current Y signal have a correlation or not.

On the other hand, the other ($Y_{2D}+C_{2D}$) signal path that is input to Pin ⑲ of IC101 (CXA1207AR) where an internal AGC circuit controls the signal level for constant amplitude. The AGC output takes another two signal paths; one output ($Y_{2D}+C_{2D}$) is added to the (Y+C) signal to produce the $(Y+Y_{2D})+(C+C_{2D})$ signal that is sent out via Pin ⑪ . (This signal is not used.)

The other ($Y_{2D}+C_{2D}$) output is sent to a subtractor where the ($Y_{2D}+C_{2D}$) is subtracted from the original signal (Y+C) to generate the $(Y-Y_{2D})+(C-C_{2D})$ signal, the signal has the nature of; $Y_{2D} \fallingdotseq Y$, $C_{2D} \fallingdotseq -C$. So, $(Y-Y_{2D})+(C-C_{2D}) \fallingdotseq 2C$ is generated, and is passed through the switch controlled by correlation detector, through a band-pass filter and output from Pin ⑬ . This signal is input to Pin ㉚ of IC121 (CXA1208R) and is hereafter used for chroma signal processing.

4-5-5. Chroma De-emphasis Circuit

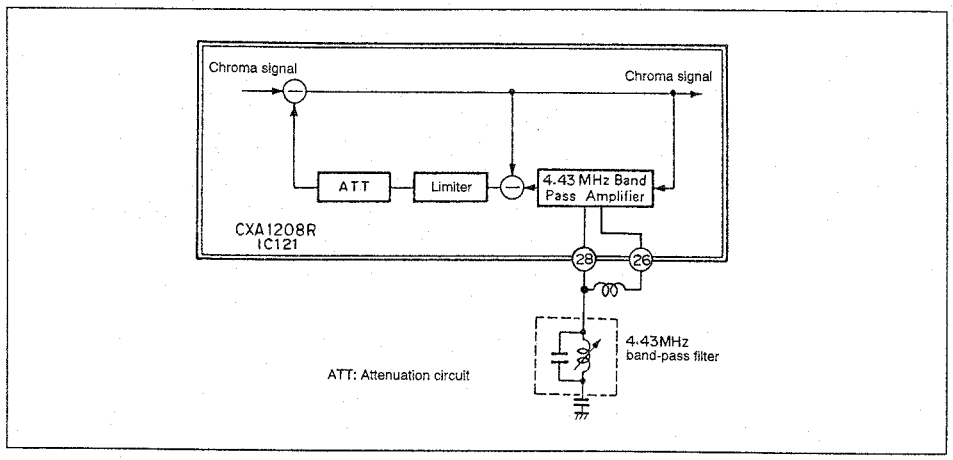


Fig. 4-54. Chroma de-emphasis circuit

The sidebands component is extracted by subtracting the signal with its sidebands component attenuated by the 4.43 MHz band-pass amplifier from the original signal at the subtractor. The resulting signal passes through the limiter and the attenuator circuit (ATT), and characteristics opposite to those used for recording are obtained by performing negative feedback to the input side.

4-5-6. Burst De-emphasis

The burst de-emphasis circuit lowers the amplification gain only during the burst signal period by the burst flag, and restores the burst signal to its original level after its gain is boosted in the burst emphasis circuit during recording.

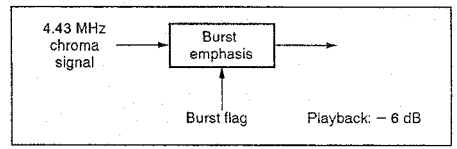


Fig. 4-55. Burst de-emphasis

4-5-7. ACK and Burst ID Circuit

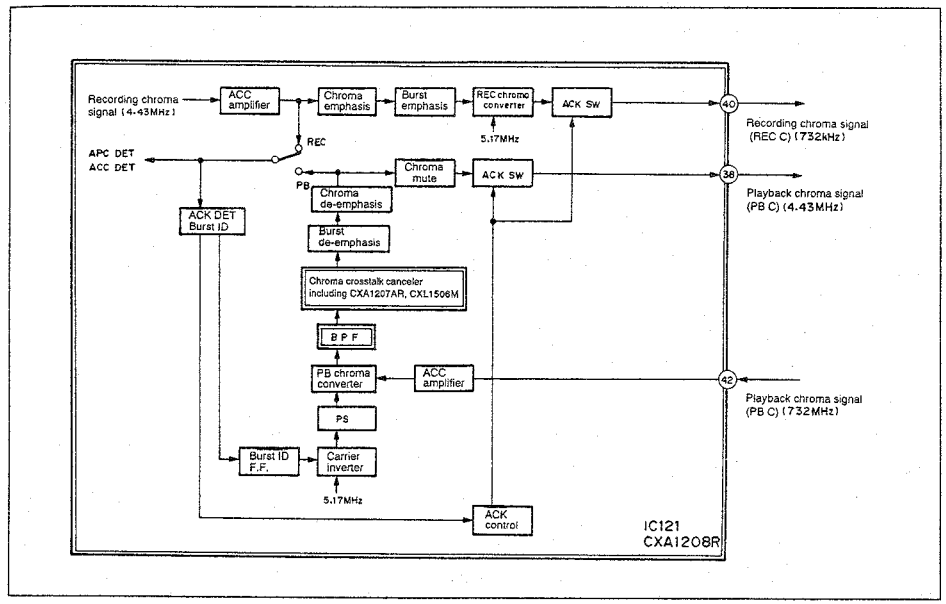


Fig. 4-56. ACK burst ID circuit

(1) Phase detection (ACK, burst ID detector)
The 4.43 MHz chroma signal and the 4.43 MHz crystal oscillator output signal, which is a reference signal, are input to the phase detection circuit. The two signals are phase-compared only during the burst period as by the burst flag signal, and the resulting signal becomes the phase detection output signal by passing through a low-pass filter.

(2) ACK detection
The phase detector output is input to the comparator and compared to the reference voltage to determine if the color or monochrome mode is set. When APC is phase-locked, the phase detector output level is proportional to the chroma signal (burst signal) level.
ACK detection recognizes the color mode when the phase detector output level is higher than the reference voltage.

Monochrome	REC	Pin ㊵ of IC121(CXA1208R): 0 Vdc
	PB	Pin ㊳ of IC121(CXA1208R): 0 Vdc

(3) Burst ID
The normal operation range of APC detection is ± 90°. Consequently, APC is not activated normally and requires longer time for repeated phase-locking when the playback chroma signal has a phase shift of more than ± 90°.
The burst ID circuit accelerates APC phase-locking inverting the chroma signal by inverting the converted carrier phase in the carrier inversion circuit when the playback chroma signal is out-of-phase by more than ± 90°.

[Burst ID detection]
When the playback chroma signal is more than ± 90° out-of-phase, phase detector output becomes negative. The F/F inversion signal is produced by the burst ID detector by comparing this output with the reference voltage.

[Flip-flop]
The flip-flop is inverted at the rising edge of the F/F inversion signal.

[Carrier inversion]
Phase of the 5.17 MHz conversion carrier is inverted by the output of flip-flop circuit.
This in turn inverts the phase of the 4.43 MHz playback chroma signal.

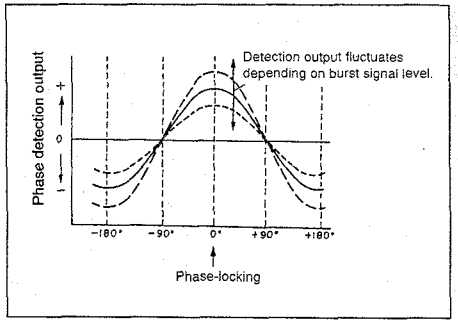


Fig. 4-57. Phase detection characteristics

4-5-8. Jog Chroma Processing
In PAL chroma signals, the R–Y signal turns every 1H. In the 8mm PAL system, colour is not aligned on the tape pattern as in the Beta PAL system. Therefore, jumping track is caused during variable speed playback(jog mode)when the playback head moves to the adjacent track and the (R–Y) and –(R–Y) sequence is lost. Correct colours are no longer played back. To prevent this, the (R–Y) and –(R–Y) sequence is detected by the burst signal, and there is selection of output of chroma signal unchanged (TH) or output of signal (DL) (obtained by frequency conversion of chroma signal by 2fsc) when the sequence is lost to playback correct colours.
The signal which has a symmetrical relationship with the TH signal (PAL playback colour signal) and B–Y axis is called the DL signal.

This VCR uses IC161 (CXA1203M) for colour alignment correction during JOG. In addition to colour alignment correction, the IC161 (CXA1203M) also has built-in SECAM DETECTOR, BELL and C-BELL filters, and can also handle PAL-M. The explanation of these functions will be omitted as they are not used.

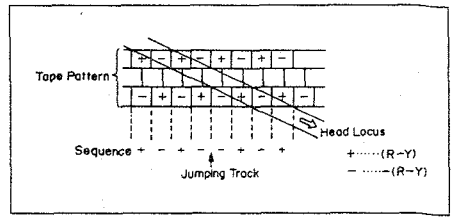


Fig. 4-58.

Block Diagram and Pin Layout

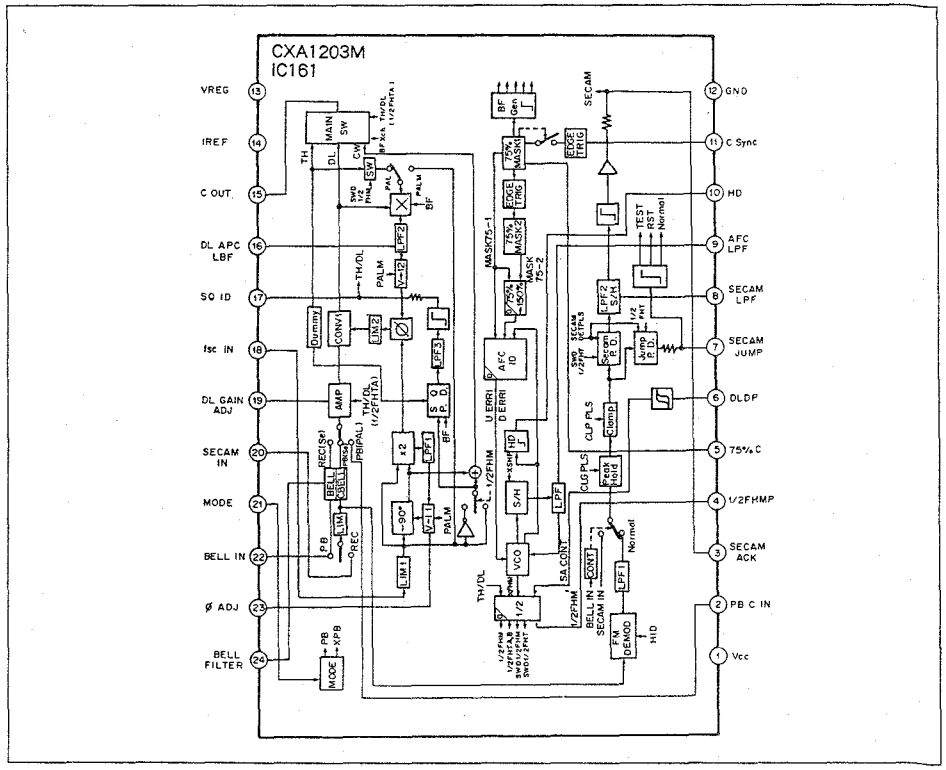


Fig. 4-59.

(1) Gain Adjust Amp. (DL signal)

This performs gain adjustment of the DL signal. The amp gain is altered by changing the DC voltage at Pin ⑲. When 5V is applied to Pin ⑲, the internal fixed gain is selected and the level of the TH and DL signals becomes the same.

(2) fsc −90° PLL
× 2
EX Burst } **BLOCK**

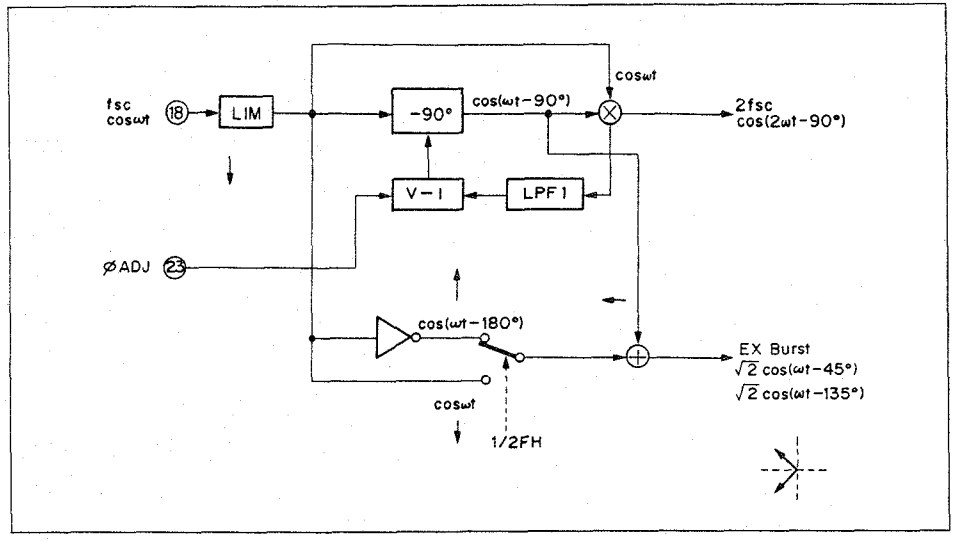


Fig. 4-60.

The fsc −90° PLL is comprised of a −90° phase shifter, multiplier, LPF1, and V→I converter, and forms a PLL loop for obtaining a signal which is delayed 90° from the fsc. The amount of phase shift is varied by changing the DC voltage at Pin ㉓, allowing for phase adjustment of the EX Burst and 2fsc duty adjustment (DC offset). The internal fixed phase shift amount is selected by applying 5V to Pin ㉓.

2fsc is obtained from the multiplier output (× 2 output).

EX burst is created by adding fsc (or inverted fsc) by the −90° delayed fsc obtained by the −90° PLL. At this time, fsc and the inverted signal are switched with the 1/2fH cycle, and the phase of EX burst changes every 1H.

(3) SQ (Sequence) DET

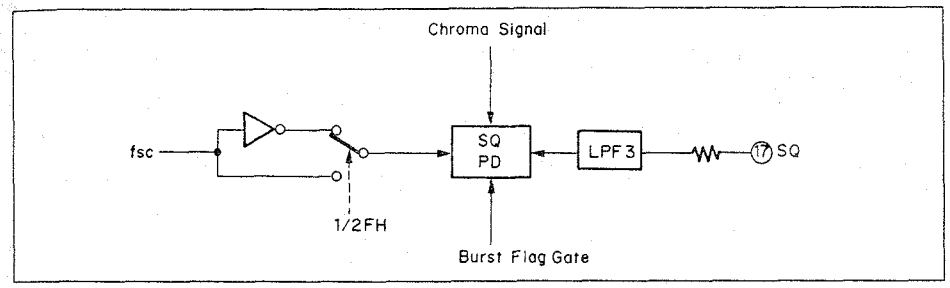


Fig. 4-61.

SQ DET detects the colour alignment of the chroma signal. SQ PD is a phase detector operating only during the burst period, and it detects the colour alignment by phase comparison of the signal obtained by inverting fsc every 1H and the burst signal of the chroma signal.

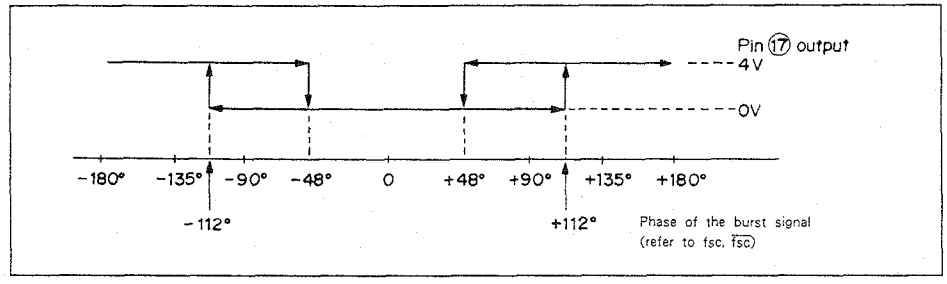


Fig. 4-62.

The above diagram illustrates the relationship between the phase of the burst signal, phase of fsc ($\overline{fsc}$), and the Pin ⑰ output (SQ). As this shows, the hysteresis angle is approximately 64°.

The proper sequence is determined when the relation is as Fig. 4-62., and the output from Pin ⑰ is set to High.

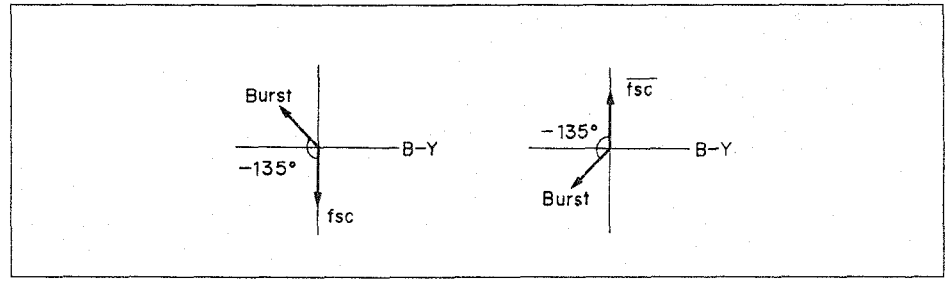


Fig. 4-63.

Thus, the burst signal central phase (B−Y axis) should have a relationship of −90° with fsc.

The Pin ⑮ output signal can be forced to TH or DL by externally fixing Pin ⑰ (SQ) to High or Low.

(4) V-Invert (V-axis inversion circuit)

In order to obtain colour alignment, it is necessary to obtain an inverted signal (DL signal) from the chroma signal (TH signal) in relation to the B–Y axis. The V-Invert BLOCK is a circuit for creating the DL signal from the TH signal. The principles are shown in Fig. 4-64.

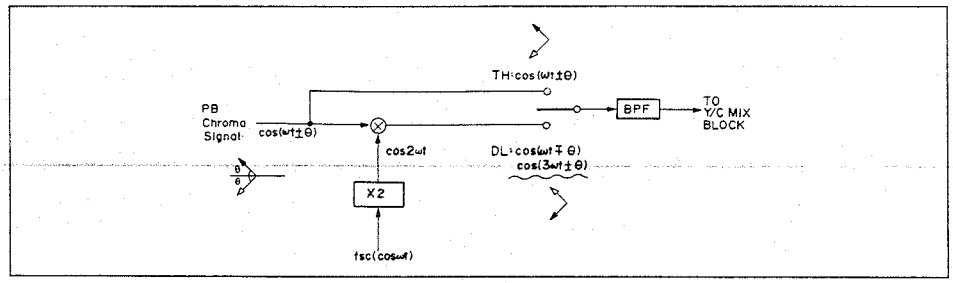


Fig. 4-64.

If the B–Y axis of the PB chroma signal is cos ω t, an inverted signal from the PB chroma signal in relation to the B–Y axis can be obtained through frequency conversion by input of this and 2fsc (cos 2 ω t) to a multiplier.

Although the tertiary component (cos 3 ω t) is also output at this time, this is eliminated by the latter-stage BPF.
The actual V-Invert BLOCK diagram is shown in Fig. 4-65.

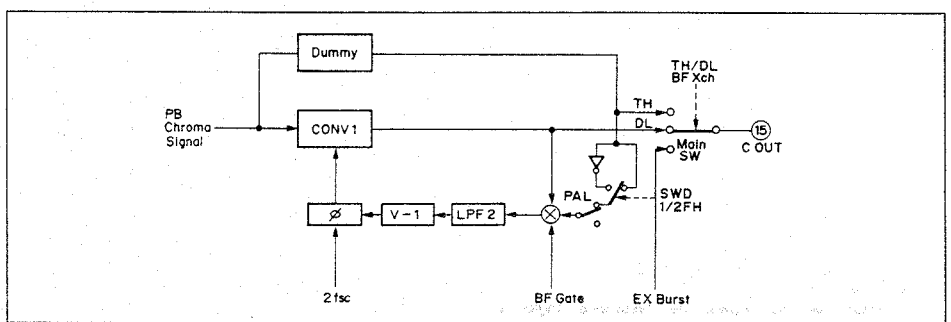


Fig. 4-65.

In addition to output of the DL signal, the V-Invert circuit forms a TH/DL APC loop which keeps the burst signals of the TH and DL signals in a 90° relationship each other. In other words, the phase of the TH and DL burst signals is detected and the amount of delay by the phase shifter ϕ is altered according to the error current. CONV1 is a multiplier for obtaining the DL signal.
The difference in gain and phase between the TH and DL signals is eliminated by Dummy giving the gain loss created by CONV1 and phase delay to the TH signal.

Main SW outputs either the TH or DL signal according to the TH/DL switching signal (Pin ⑰ output). EX burst is output by the BF Xch pulse (only during JOG).
Mode selection is performed by the voltage at Pin ㉑. The table 4-4. illustrates the relationship between the voltage at Pin ㉑ and the MODE.

Pin ㉑ Voltage	Mode
0 to 1.3V	REC
1.7 to 2.8V	PB
3.2 to 5.0V	JOG

Table 4-4.

(5) fH PLL

AFC ID performs frequency comparison of C sync and the VCO oscillation frequency, an up or down error is detected when there is a frequency difference, and the VCO oscillation frequency is set to the vicinity of 15.625 kHz. If the error continues for a period of 15H × 6 (= 5760 µsec), an AFC ID is output.

The AFC ID also performs SYNC loss detection, and the status immediately before AFC ID output switching off is held when there is C sync loss by variable speed playback, etc. The phase (frequency) lock of C sync and the VCO oscillation frequency is performed by the PLL loop formed by S/H and the LPF.

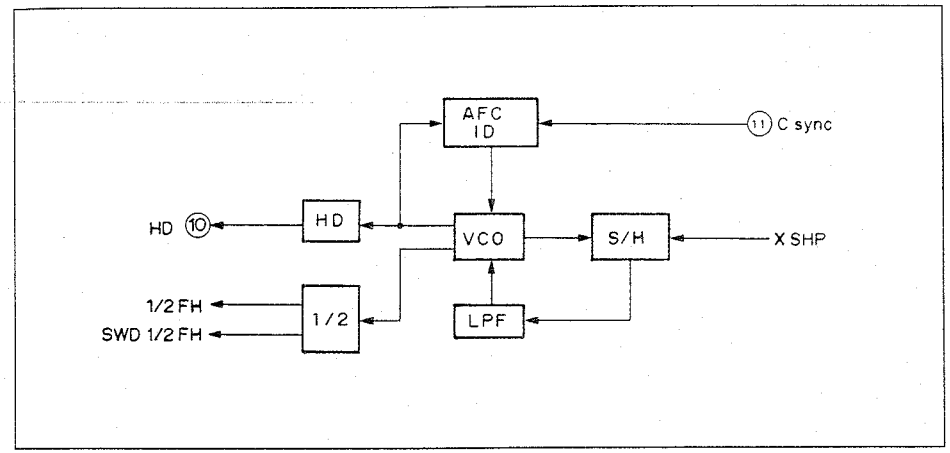


Fig. 4-66.

5. AUDIO CIRCUIT

5-1. OUTLINE

There are four types of audio recording systems.

1. FM Audio (monaural)
2. FM Audio (stereo)
3. PCM Audio (stereo)
4. AUX Audio (monaural)

Of the above four types, FM audio (monaural) is indispensable while FM audio (stereo), PCM and AUX are optional.
This equipment uses only FM audio (monaural).

[FM audio (monaural) standards]

	Standards	Remarks
Carrier wave frequency fA	1.50 ± 0.02 MHz	
Maximum frequency deviation Δ f	± 100 kHz	
Recording current IA/IC	–13.0 ± 2.0 dB	Set chroma signal recording current at 0 dB.
Noise reduction	Refer to section on "Noise reduction".	
Recording FM signal band width	1.50 ± 0.15 MHz	Band width including 99% of the entire spectrum component (power factor)
Standard frequency deviation	± 60 kHz	Modulation frequency 400 Hz

Table 5-1.

[Noise reduction standards]
The noise reduction standards of FM audio (monaural and stereo) and PCM audio are the same for this equipment.

		Standards	Remarks
Pre-emphasis		Fixed	
Compression ratio		2	
Time constant	Pre-emphasis 1	75 µsec, 19 µsec	2.12 kHz, 8.38 kHz
	Pre-emphasis 2	75 µsec, 27 µsec	2.12 kHz, 5.89 kHz
	Waiting	75 µsec, 27 µsec	2.12 kHz, 5.89 kHz
Transient characteristics	Attack time	3 msec	Tolerance ± 20%
	Recovery time	40 msec	
	Hold time	15 msec	
Frequency characteristics (when recording)		Refer to "Frequency characteristics".	Standard input level
Linearity		Refer to "Noise reduction I/O characteristics".	

Table 5-2.

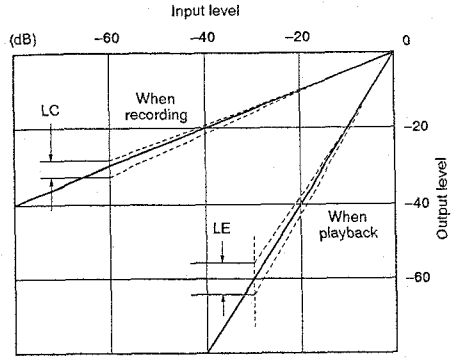
[Frequency characteristics···when recording]

Frequency (Hz)	50	100	200	400	700	1k	2k	4k	7k	10k	14k
Response characteristics (dB)	0	0	0	0	+0.1	+0.3	+1.2	+2.7	+4.1	+4.8	+5.3

Tolerance ± 1.5 dB

Table 5-3.

[Noise reduction I/O characteristics]



LC: Linearity tolerance when recording (compressor) ± 1.5 dB

LE: Linearity tolerance when playback (expander) ± 3.0 dB

The audio circuit is on the CP1 board. IC201 and LA7454W as monolithic IC play a important role of the circuit .
The earphone terminal is provided on the PW1 board.

5-2. RECORDING SYSTEM

5-2-1. Microphone Circuit

The tone of the built-in microphone signal is compensated by the tone compensation filter Q2801. Lower range tone is compensated at C2802 and higher range tone at C2821 and C2834.

5-2-2. Microphone Amplifier Circuit (Hereinafter Referred to as CP1 Board)

The microphone amplifier is composed of the transistor Q2831 and Q2832 to amplify the microphone signal by 28 dB. REG 4.2V of IC201 is used for the power source of the microphone circuit and for bias of the microphone amplifier.

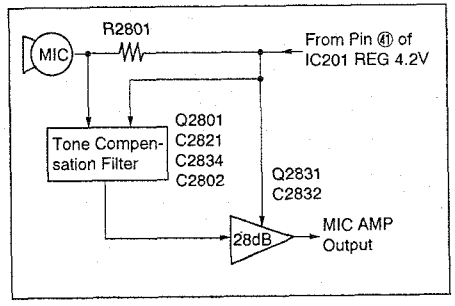


Fig. 5-1. Microphone and MIC amplifier circuit

5-2-3. Input Selection, ALC Circuit

Audio input consists only of input of the built-in microphone and amplified signal is input from Pin ㊳ of IC201 to the ALC circuit by the microphone amplifier. (Pin ㊲ is normally High and microphone amplifier output is selected).

The ALC circuit keeps excessive input to a certain fixed value by detecting the output of the ALC amplifier with the ALC detector and performing feedback control of the ALC amplifier using DC voltage proportional to the input signal. The ALC transient response (attack time and recovery time) is determined by the CR of Pin ㊵.

During microphone input, recovery time is shortened by strengthening the gain for maintaining of a wide coverage range of 22 dB by sound erasure.

5-2-4. Mute and Low-pass Filter Circuit

The output of ALC is fed to the low-pass filter (LPF) through the R/P switch and the mute circuit.

The mute circuit mutes the audio signal when the mute signal is sent to Pin ㉞ from the SYSCON.

The LPF is a tertiary active filter built into the IC. It eliminates the unwanted band above 30 kHz to prevent erratic noise reduction at a later stage.

In the PAL system the control signal input to Pin ⑬ is fixed to High and LP emphasis is not performed.

With this model the voltage of Pin ③ is fixed at 0.5% the accuracy of R.

The demodulation sensitivity of the PLL demodulator coincides with the modulation sensitivity of the VCO. Therefore, if the demodulation sensitivity is adjusted (fixed at R) at Pin ③ during playback, adjustment of recording time is performed at the same time.

Since in the PAL system ⑬ is fixed to High, PAL is fixed to SP.

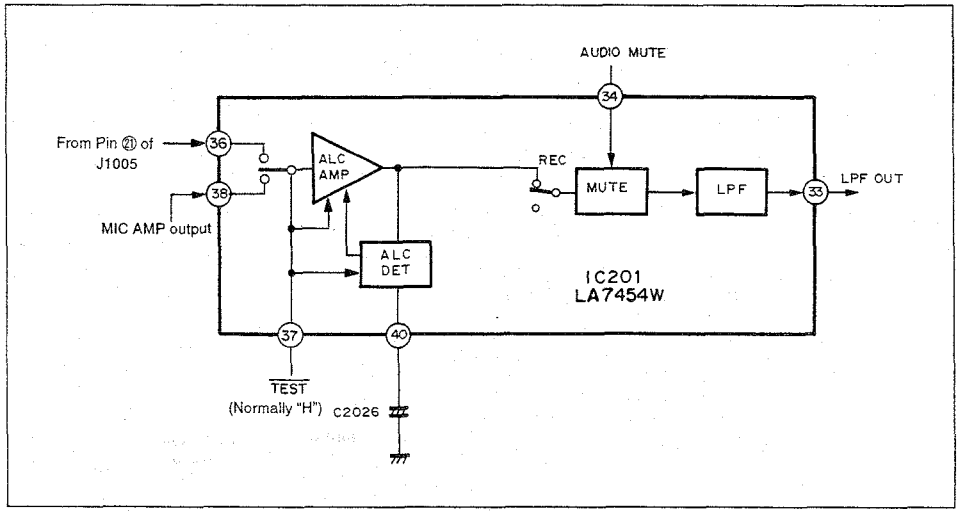


Fig. 5-2. From ALC to LPF circuit

5-2-5. Noise Reduction Circuit (REC)

The output of the LPF is output from Pin ㉝ and then fed to Pins ㉜ and ㉛. The output of Pin ㉜ is sent to the line output and the earphone terminal as a monitor output.

The audio signal of Pin ㉛ is fed to the + side of the MOA (Main Operational Amplifier) of the noise reduction circuit via R/P switch.

An emphasis circuit for the somewhat reduced high band is inserted in the negative feedback loop of the MOA. The output of the MOA is therefore subjected to pre-emphasis what elevates the band to a higher band. Further, as the feedback amount is either increased or decreased in proportion to the input level by the VCA (Voltage Control Amplifier), the feedback amount of a large input level increases and the output is held and that of a small input level decreases and the output is increased. For this reason, the dynamic range (a difference between a large level and a small level) of the audio signal is compressed.

When the higher band component only of the audio signal is input, the gain of the VCA is increased by waiting. Therefore, emphasis 2 is canceled, and the amount of emphasis is held, thereby preventing the pre-emphasis from becoming too large. The waiting and the emphasis 2 are primary filters of reverse characteristics. These are mounted in the IC. Because the relative brightness in the IC is good enough, perfect reverse characteristics can be realized.

The transient response of the noise reduction circuit is determined by the capacitor at Pins ㉖ and ㉗, and the attach/recovery time is determined by Pin ㉖, and the hold time by Pin ㉗.

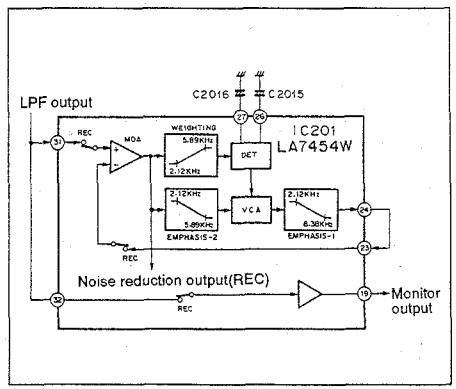


Fig. 5-3. Noise reduction circuit (REC)

5-2-6. LP Emphasis Circuit (REC)

The output of the noise reduction circuit is fed to the operational amplifier for the LP emphasis via R/P switch.

The LP mode of NTSC is only 10 µm in track width, which makes impossible to secure the sufficient signal-to-noise ratio merely with the emphasis of the noise reduction circuit. The LP emphasis is therefore added.

During the recording operation, pre-emphasis is applied because the emphasis time constant is inserted into the feedback loop of the operational amplifier. A resistor is mounted in the IC, and the capacitor is connected to Pin ⑭. In the PAL system, the control signal input to Pin ⑬ fixed to High and LP emphasis is not performed.

5-2-7. Limiter Circuit

The amplitude above a certain level of the output of the LP emphasis is clipped by the LIM (limiter) via Pins ⑮ and ⑯, and prevented from being an over-modulation by the next-state modulator to avoid interference on the video image.

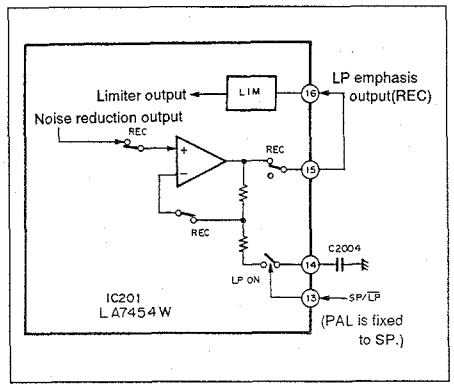


Fig. 5-4. LP emphasis (REC)

5-2-8. VCO Circuit

The output of the limiter is level adjusted by the VCA via R/P switch to become an FM wave in the VCO and then output from Pin ⑧.

The modulation sensitivity (frequency deviation) is determined by setting the gain of the VCA with the DC voltage at Pin ③.

With this model the voltage of Pin ⑥ is fixed at 0.5% the accuracy of R.

The VCO is composed by making the variable BPF a forward loop of a gain above 1. The Pin ⑧ output is a sine wave because the output signal is output from the output end of the BPF.

The oscillation frequency becomes the center frequency of the variable BPF, and it is made the FM modulation (VCO). The FM center frequency (fo) is determined by the DC component of the control signal, and the frequency deviation (Δ f) by the AC component. The free-run frequency of the VCO is adjusted by the DC voltage at Pin ㊺. The filters (VCO, BPF, LPF, WE, and EMP2) mounted in the IC are determined by the DC voltage at Pin ㊺ in all cases. When the below-mentioned BPF is adjusted, other filters are automatically adjusted to the target values because the relative accuracy inside the IC is high.

5-2-9. fo PLL Circuit

In the free-run frequency of the VCO, the fo stability of ± 10 kHz cannot be obtained under any environmental conditions, fo is stabilized through PLL automatic control using the clock of crystal accuracy. fsc is used for the clock signal. The fsc/N with the fsc frequency divided to the extent of N, and fo/M with the fo frequency divided to the extent of M are fed to the phase comparator (ϕ COMP), and phase difference is smoothed by the loop filter at Pin ㊼ to become a DC control signal for feedback to the VCO. Therefore, the fo/M always follows the fsc/N for phase lock to become the same frequency.

Therefore, there is no difference between fo/M=fsc/N and fo=(M/N)fsc. Here, M=8208, N=19584 (NTSC), and 24192 (PAL). An N frequency divider switchover between NTSC and PAL is so made that a switchover is made to the NTSC system when Pin ㊸ is pulled up by an external resistor and that a switchover is made to the PAL system when it is open (pulled down by the internal resistor).

This pull-up resistance consists in the VDI board.

The loop filter of Pin ㊼ is set to a large time constant to avoid adverse effects on the audio signal. If nothing is done to preclude the possibility, the considerable pull-in time is needed at the time of power on. The time constant is made 1/10 for facilitated pull-in by the mute signal of Pin ㉞ inside the IC at the time of power on and during a mode switchover from PB to REC.

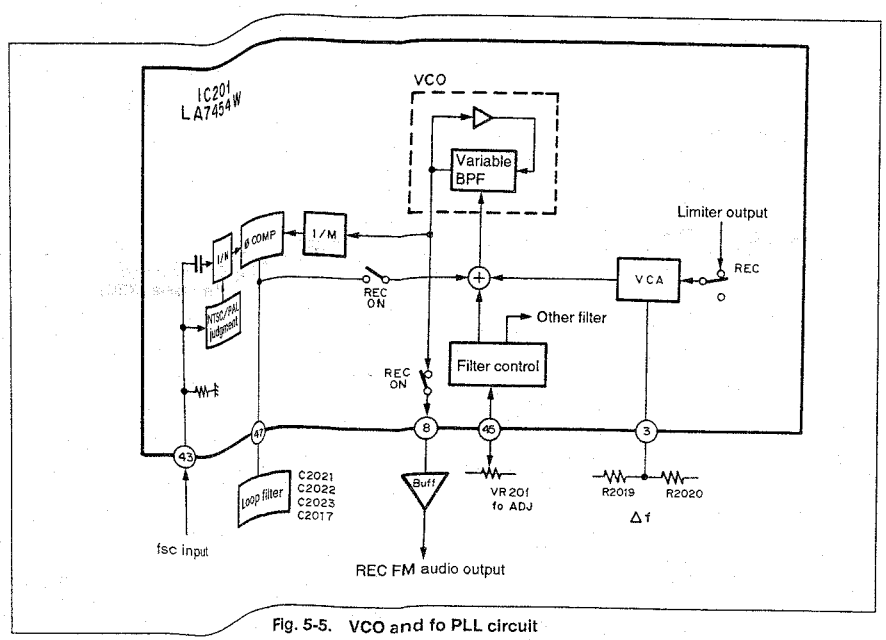


Fig. 5-5. VCO and fo PLL circuit

5-3. PLAYBACK SYSTEM

5-3-1. FM AGC, BPF, and Limiter

The signal played back by the video head is amplified by the IC191 and fed to Pin ① of IC201.

The RF signal fed to Pin ① is set to the uniform head output by the FM AGC, and a 1.5 MHz audio FM signal is extracted by the internal BPF. The output of BPF can be monitored with the signal from Pin ④ (TP201). While playing back the standard tape, when the amplitude levels of the higher frequency and the lower frequency of FM wave of the output from this pin become the same, the center of BPF becomes 1.5 MHz. The IC built-in filter adjustment can be performed in this state. The control signal of the AGC is derived from the output of the BPF so that the AGC serves to make the 1.5 MHz component constant at a certain level.

The time constant of the AGC is set by the capacitor of Pin ㊽.

The AM component of audio FM signal extracted by the BPF is completely eliminated by the limiter (LIM) and sent to the FM demodulator.

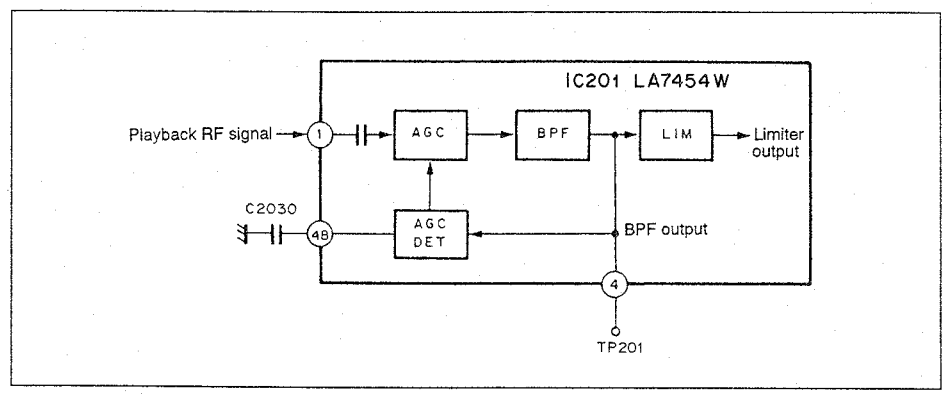


Fig. 5-6. FM AGC to Limiter Circuit

5-3-2. FM Demodulator

The FM demodulator consists of a VCO and a VCA used as an FM modulator at the recording operation and is formed as PLL circuit.

The FM audio signal and the VCO output is fed to the phase comparator (ϕ COMP), and the carrier component is eliminated from the phase error output by the loop filter at Pin ⑥. It is then set in amplification by the VCA via R/P switch and fed back to the VCO. Therefore, the VCO is phase locked to the audio FM signal to follow it. At that time, the control signal of the VCO becomes a demodulated audio signal.

The demodulation sensitivity of the PLL demodulator coincides with the modulation sensitivity of the VCO. Therefore, if the demodulation sensitivity is adjusted (fixed at R) at Pin ③ during playback, adjustment of recording time is performed at the same time.

The demodulation sensitivity of the PLL demodulator coincides with that of the VCO. The demodulation output of Pin ⑥ is DC unstable, and the DC bias is given by R2001.

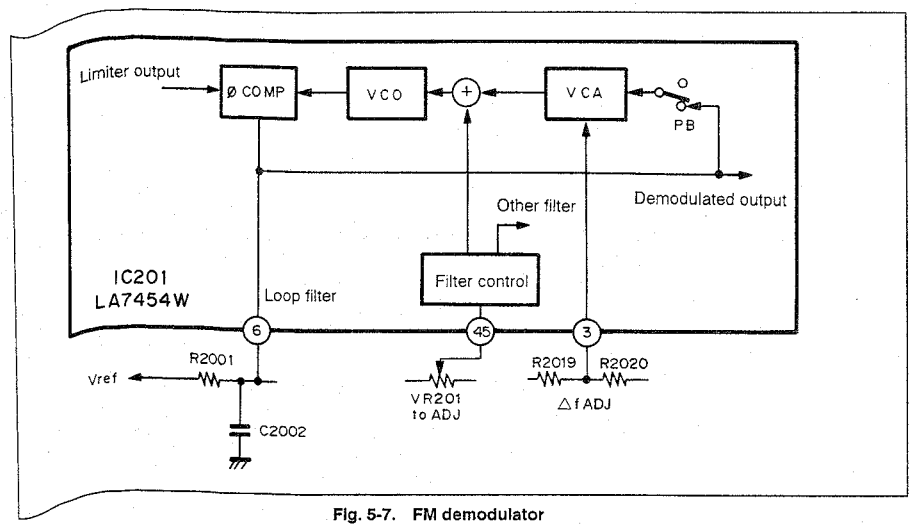


Fig. 5-7. FM demodulator

5-3-3. S/H (Sample and Hold) Circuit

At the time of head switchover and dropout generation, spike noise appears at the demodulated output. It must therefore be eliminated by the sample and hold circuit. At the head switchover point, wow and flutter occurs. The FM wave is not continuous for that reason, and the phase changes in a stepped fashion. Since the time differential of the phase is the momentary frequency, that is, the demodulated output, it becomes spike noise. The time width of the spike noise depends upon the demodulation band. That is, wider the time width, shorter the time becomes. Because the demodulation band is set for a broader range to hold the spike noise, i.e., the hold time width to a minimum, considerable FM wave remains in the demodulated output. If the hold is done directly, erratic hold may result. To preclude this possibility, the average value hold circuit is adopted to ensure the "hold" at the 5 μ sec hold time and at the center value of the audio signal. The hold pulse at the head switchover point is generated at the edge of the RF SW1 (30Hz) of Pin ⑩ by the PG doubler.

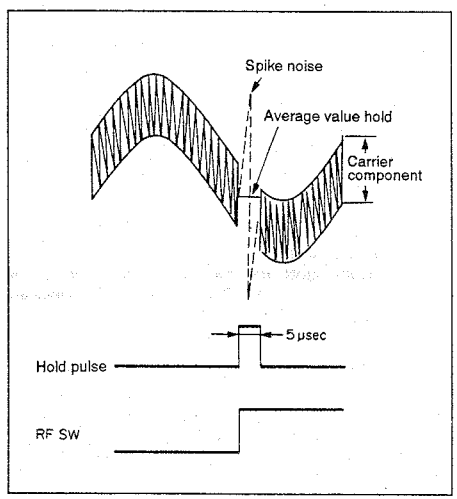


Fig. 5-8. Sample and hold circuit waveform diagram

5-3-4. Dropout Detection and Mute Detection Circuit

The FM audio signal extracted by the BPF is level detected by the dropout detection circuit (DO DET), but at the time of dropout generation, the DO hold signal is sent to the S/H circuit for holding. The pulsewidth of the DO hold signal is detected by the mute detection circuit (MUTE DET). After a certain period of time (500 μsec), the mute signal is output. The judgment time is determined by the capacitor of Pin ②.

The mute signal once turned on is held for a certain period of time (about 150 msec) by the off delay circuit even if the DO mute signal is turned off. The off delay circuit is so designed that nine pieces of shift registers serve to make the hold pulses at the point of head switchover clocks, thereby causing the power off of the DO mute signal to be delayed.

A function such as this prevents an audio signal from being sent out when the dropout is consciously generated over a relatively long period of time, just as in the case of playback of clogged one side head. The timing chart for dropout compensation is shown in Fig. 5-9.

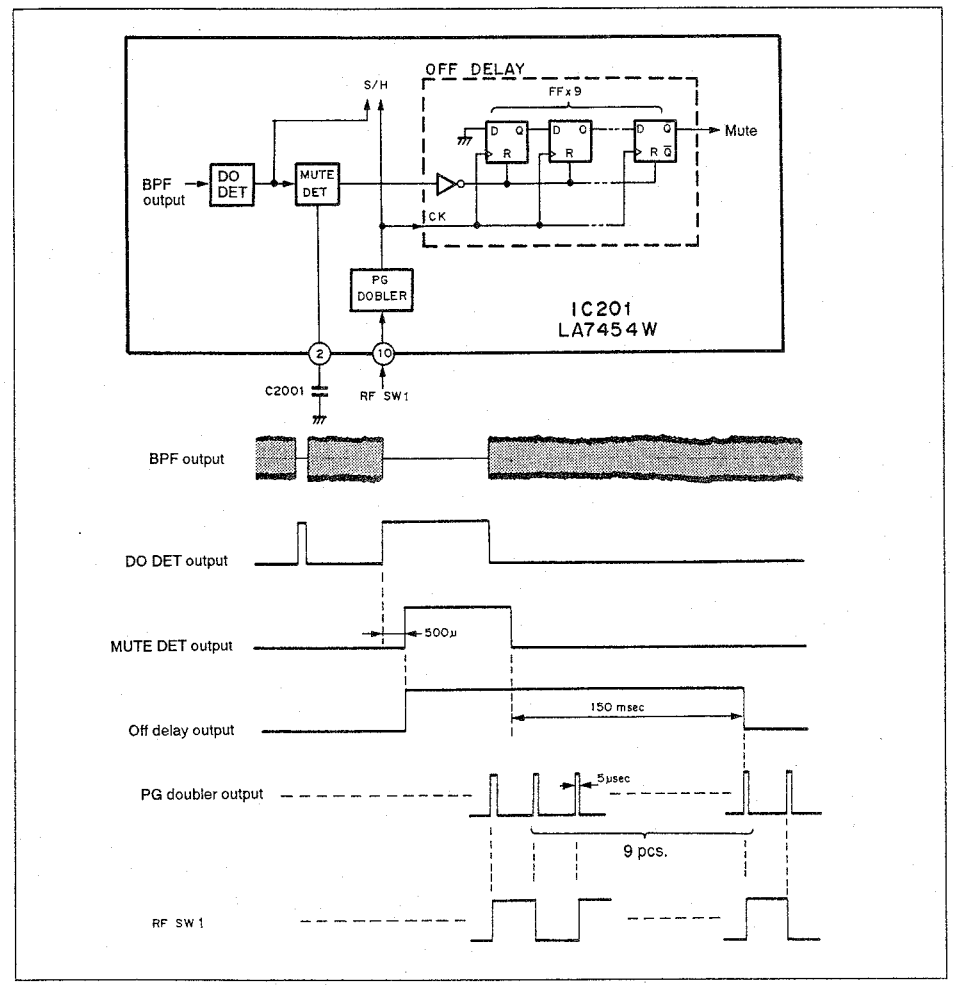


Fig. 5-9. Dropout detection and mute detection circuit

5-3-5. LP Emphasis Circuit (PB)

The demodulated output is subjected to noise rejection by the sample and hold circuit and fed to the operational amplifier for LP emphasis via R/P switch.

The operational amplifier serves merely as a buffer during the playback, and the constant is an open circuit during the emphasis, performing the de-emphasis operation. The LP emphasis output is output from Pin ⑮ via R/P switch and fed once again to Pin ⑯.

Since in the PAL system Pin ⑬ is fixed to High, LP emphasis is not applied to it. Pins ⑮ and ⑯ can be checked for modulated input during the recording and demodulated output during the playback.

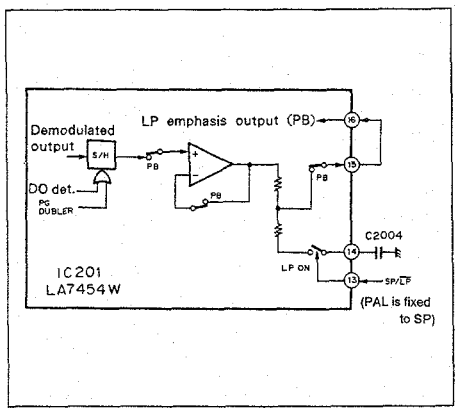


Fig. 5-10. LP emphasis circuit (PB)

5-3-6. Mute Circuit and LPF Circuit

The audio signal fed to Pin ⑯ is passed through the mute circuit and the LPF circuit via R/P switch and output from Pin ㉝.

In the mute circuit, the audio signal is muted by the control signal sent to Pin ㉞ from the SYSCON during the special playback and the mute signal during generation of a dropout of longer than 500 μsec.

In the LPF, spurious band above 30 kHz is eliminated, to prevent erratic operation of the next-stage noise reduction circuit from occurring.

5-3-7. Noise Reduction Circuit (PB)

The audio signal output from Pin ㉝ is fed once again from Pin ㉜ and then fed to the MOA of the noise reduction circuit via R/P switch.

The MOA during the playback becomes a mere buffer, and the emphasis circuit and the VCA circuit previously in the feedback loop during the recording serve as open loop circuits. Therefore, the de-emphasis and extension just the reverse of those during the recording are made.

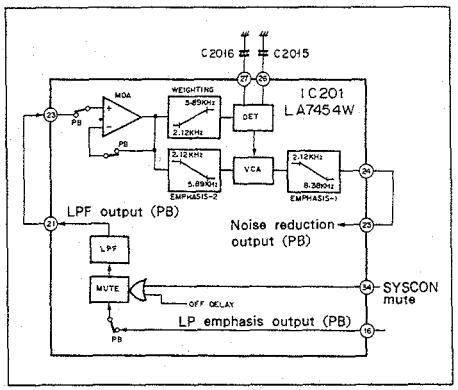


Fig. 5-11. Noise reduction circuit (PB)

5-3-8. Output Circuit

The noise reduction output is fed once again to the IC from Pin ㉓, amplified to –7 dBs by the line amplifier via R/P switch, and then output from Pin ⑲. The line amplifier has the capability to drive the earphone directly. The line output and the earphone output can be driven from the same amplifier.

A shunt switch is built in Pin ⑱, and shorting is done to the ground by the mute signal of Pin ㉞, utilizing the output resistors of the line. By so doing, the shock sound is held when the power is ON and OFF.

The line amplifier has large amplitude level and large power consumption during the earphone drive. The power is supplied to it from Pin ⑰, which is something different from other circuits.

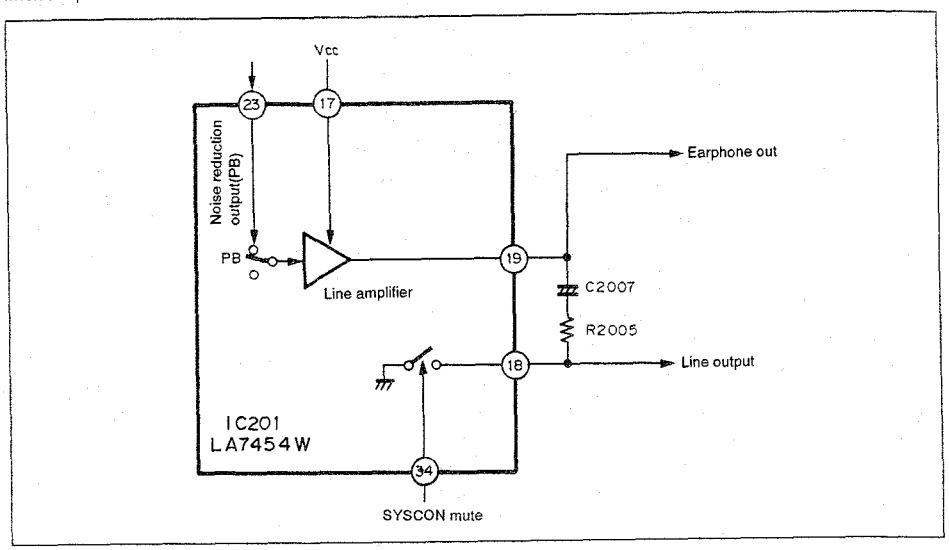


Fig. 5-12. Output circuit

6. SYSTEM CONTROL CIRCUIT

6-1. GENERAL

6-1-1 Compositions and Functions

For the whole composition of system control, refer to the block diagrame in 4-3 "Service Manual".

The system control circuit is designed around the following microprocessor.
Main controller IC351 (CXP80720) (CP1 Board).

The main controller performs the following functions:

1. Operation key-in.
2. Character display on the CRT screen.
3. Clock control.
4. Settig electronic shutter speed for the camera.
5. Power ON and OFF.
6. Backup of clock, counter and shutter speed data.
7. Mode control: Control for the whole system of actuation mode.
8. Mechanism control: Detection of mechanical condition, and sequence control for loading and capstan motors.
9. Circuit system control: Control of video, audio and camera circuits.
10. Servo control: Servo control of drum motor and tape running control by capstan motor.

The above functions are shared respectively.

For more mention about the servo control, described in the next section No.7.
About functions on each terminal of the main controller IC, arranged in the diagram at the later section (6-10).

6-1-2. Inner Bus Communications System

The system control circuit controls the deck in its entirety by detecting the key-in operation, and the internal mechanism inside the deck, and the signal system circuit status. Information input from all sensors is read into a microprocessor, namely, the main controller, and processed, after which it is sent out as operation mode setting information to mechanisms such as the motor, signal processor circuits such as the video, audio and camera signal processing circuits, and display units such as the viewfinder. In addition to the parallel signal line, bus lines for serial transmission are provided for transmission of information among the main controller and various signal processing circuits.

Four ICs are linked by serial buses shown below.

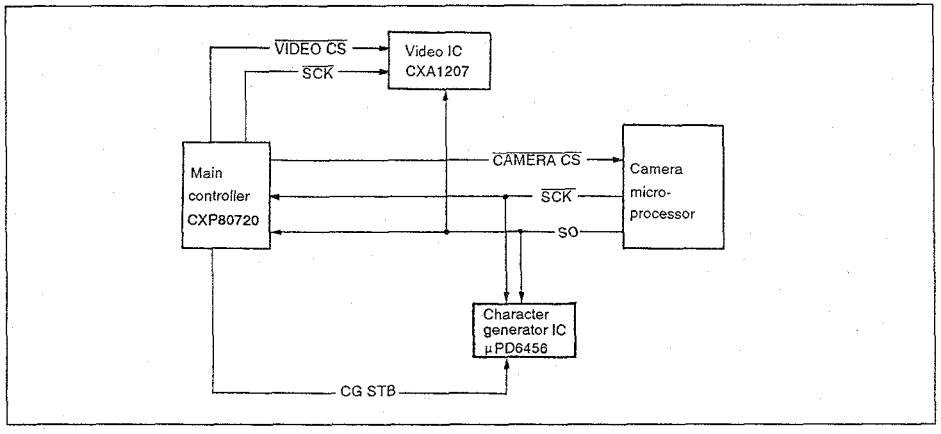


Fig. 6-1. Inner bus communications system

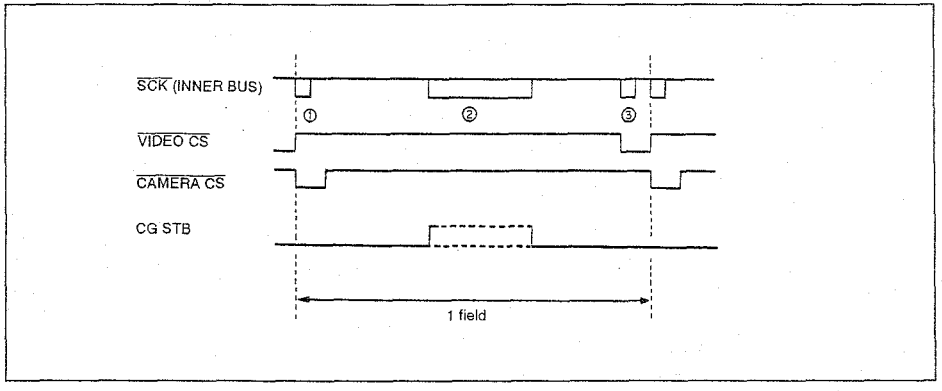


Fig. 6-2. Inner bus signal timing chart

	Inner Bus	Clock Output	Clock Cycle
①	Main controller → Camera microprocessor	Camera microprocessor	2 bytes/1 field
②	Main controller → Character generator IC	Main controller	16 to 24 bytes/1 field
③	Main controller → Video IC	Main controller	3 bytes/1 field

Table 6-1. Inner bus signal specifications

6-2. KEY-IN

The command of actuation mode for deck can be also performed by remote controller in addition to being done by the operation key on the main unit.

6-2-1. KEYs of Main Unit

Key-in operation is processed by the Main-controller.
Keys are arranged on the 3 × 4 matrix circuit.
For methods of operating keys, refer to "Instruction Manual".

Function	Uses
PLAY, STOP, FF, REW, STILL, START/STOP, EJECT, SCENE+, SCENE –	VTR operation key
CAM PW ON, VTR PW ON, STAND-BY	POWER operation key
TIME_ADJ, DATE/TIME	Clock operation key
CNT_RST, CNT_MEMO	Tape counter operation key
ZOOM TELE, ZOOM WIDE, PRESET, AF/MF, MF+ , MF – , AUTO LOCK	Camera related operation keys
ADJ	Adjusting mode setting

Table 6-2. Switch functions/uses

IN / OUT	$\overline{\text{SCAN IN 0}}$	$\overline{\text{SCAN IN 1}}$	$\overline{\text{SCAN IN 2}}$	$\overline{\text{SCAN IN 3}}$
$\overline{\text{SCAN OUT 0}}$		MF+	PRESET	SCENE –
			STOP	REW
$\overline{\text{SCAN OUT 1}}$	AF/MF	MF –	SP/LP	SCENE+
	STILL		PLAY	FF
$\overline{\text{CAMERA CS}}$	ZOOM WIDE	ZOOM TELE		

Table 6-3. Operating key matrix Top: During CAMERA/Bottom: During VTR

6-2-2. Remote Controller

The remote operation is possible by using the remote controller (IR remote controller) by infrared rays. Input signals (REMOTE), changed into electric signals in the remote control detector (CP1 board), are input to the main-controller (Pin ⑮).

The length of 1 data block is 108 msec and only at the first when the key is pressed, the code data according to the key is issued, hereafter, the fixed code when locked is repeated in the key state locked (continuously pressed).
The main controller decodes the received serial data and makes the same process as key input of the deck side.

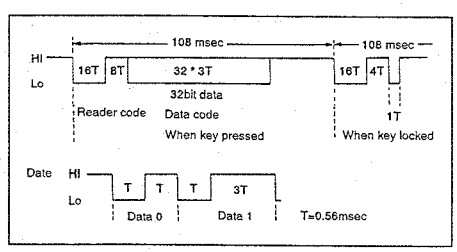


Fig. 6-3. Protocol of remote controller data

6-3. DISPLAY CONTROL

Various characters are displayed on the viewfinder to display the operation mode of the deck.
Displaying forms and contents on the screen are summarized in a table in the later section 6-11.
Refer to the "Instruction Manual" as well.

6-3-1. Screen Character Generator Circuit

To display characters on the screen, the display control data is transmitted from the main controller, via the serial bus, to the character generator circuit where character signals are created.
The character signal created is superimposed on a video signal in the video circuit.
The composite sync signal (COMP_SYNC) separated from the video signal is input to Pin ⑯ of the main controller (IC351). The vertical sync signal ($\overline{\text{CG VD}}$) for creating character signals is created in the main controller, and output from Pin ⑦. After signals regulated as signals without time axis modulations are output from the viewfinder circuit, the horizontal sync signal is input to the character generator circuit IC325 together with $\overline{\text{CG VD}}$. The character signal and the fringe signal of the character to be superimposed on the video signal are created in IC325 according to the serial data (Pin ③ input) transmitted from the main controller.
Character signals consist of those for displaying on the viewfinder like the operation mode display, and those recorded on tapes like dates and time. As IC325 has two systems for outputting the character signal, signals for displaying and signals for recording are output from separate terminals. Data for displaying ($\overline{\text{OS\_DISP\_DATA}}$) and its fringe signal ($\overline{\text{OS\_DISP\_BLNK}}$) are output from Pin ⑬ and Pin ⑭ respectively. Data for recording (CG_REC_DATA) and its fringe signal (CG_REC_BLNK) are output from Pin ⑪ and Pin ⑫ respectively.
Refer to the chapter on video circuit for details on superimpose processing.

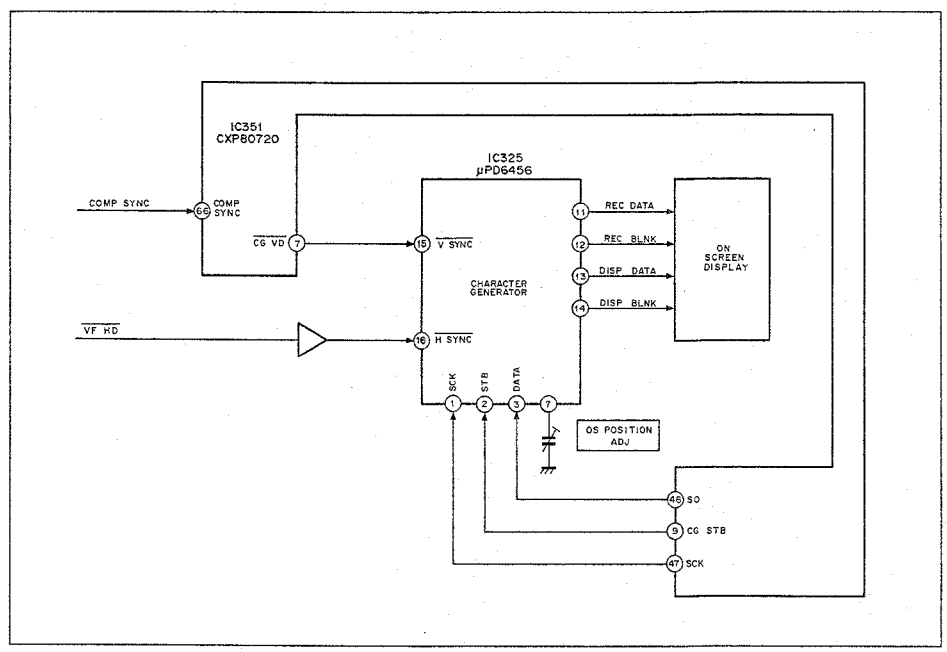


Fig. 6-4. Screen character generator circuit

6-3-2. Clock Function and Display

The main controller contains a clock function. The display of time and date is made by reading this clock data.
This clock is designed to continue its operation on the backup lithium battery mounted in the deck even when the battery is removed.
Also, a delicated crystal oscillator is provided as a clock source for increasing the accuracy of time-keeping.
To attain high clock precision, an exclusive crystal oscillator for the clock is provided separately as a microprocessor clock.
The control of date and time display is made by two keys, DATE ON/OFF and TIME ADJ.
For details on key operation procedure, refer to the instruction manual.

6-3-3. Linear Tape Counter Display

The amount of tape travel is displayed on the counter by calculating the amount of rotation of the capstan motor. The number of rotation pulse (CFG) of the capstan motor is converted into the tape recording time and then displayed. The data detected by the main controller is sent to the timer controller.
Use the CNT RESET key to clear the counter display data to 0.
For further details on operation procedure, refer to the Instruction Manual.

6-3-4. Camera Focus Selection

The selection of camera focus is made by the $\overline{AF}$/MF signals sent from the camera block to the sub controller.
The focus mode selected is displayed in the viewfinder.

6-4. CAMERA PRESET MODE SELECTION

The PRESET key is used for setting the camera preset mode in the main controller.
A signal corresponding to the selected preset mode will be transmitted to the camera section as a serial signal.
Refer to the "Instruction Manual" for details on setting.

6-5. CONTROL OF VIDEO AND AUDIO CIRCUITS

The mode select signal and timing switchover control signal are sent to the video and audio circuits. Refer to the block diagram in the Service Manual. For signal specifications, refer to the appropriate sections of the video circuit and the audio circuit system descriptions. The timing signals are in most cases synchronized with the rotation of the drum motor. For information about the timing of these, refer to the appropriate section of the servo system and the video circuit system description.

6-6. POWER CONTROL

For details on the power system of whole the deck, refer to the block diagram in the Service Manual.
The following is a description of the power start up and switchover processings in the system controller.
Voltage is applied to most circuit systems in normal operation (when the power is on) from two DC/DC converters (DDC) of the VTR section and that of the camera section.
To the system control circuit and the servo circuit, UNREG voltage directly from the battery, and the regulated ALWAYS +5V as well, are supplied. With the battery removed, the voltage from the lithium battery is supplied to the sub controller for backup of the clock program operation and also just to be ready for deck starting.
The IC335 (S-8420) includes a power controller function.
It creates ALWAYS +5 from the UNREG voltage (Pin ⑧ input/Pin ⑦ output). Moreover, it is also equipped with a circuit which switches to the lithium battery for backup when the battery is removed.
A signal indicating that the battery has been removed ($\overline{BATTERY\ OFF}$) is generated at this time.

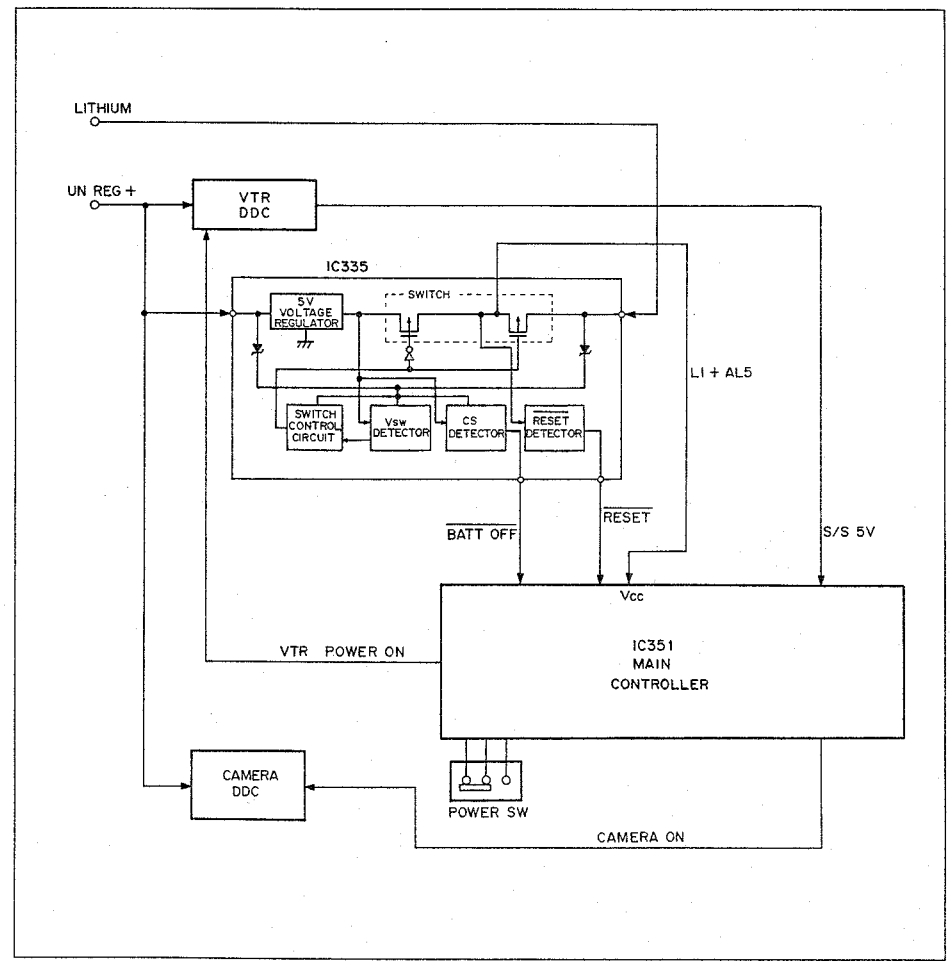


Fig. 6-6. Block diagram of power control circuit

6-6-1. Power ON Processing

When the battery is removed, the main controller operates in the sleep mode on the lithium battery for backup. In this mode, the clock oscillator supplies a 32 KHz clock.
In this condition, the main controller only scans the battery-on-signal ($\overline{\text{BATTERY OFF}}$, Pin ㉒ input).
When the battery is loaded and $\overline{\text{BATTERY OFF}}$ becomes high, the main controller is set from the sleep condition to the active condition. Key scan begins, and the position of the power switch is determined.
The mode to be set next will depend on if the power switch is at the on position or is still at the VTR side/camera side.
If at "on", the DDC at the VTR side is started up, and the VTR ON is made high to set all circuit systems into the active condition.
When the switch is at the camera side, the PAUSE mode is set. When at the VTR side, the STOP mode is changed to the initial shift mode.
When the battery is loaded, the main controller will be in the active condition by the ALWAYS+5 voltage, and perform key scanning even if the power is off.
In whichever case, it will automatically be set into the holder up mode if the cassette holder is raised. However, it will shift into the STOP mode if the cassette is not loaded, the claws are broken (record prohibition), at tape end, or when dew has occurred.

6-6-2. Power OFF Processing

Power Off processing begins when the power switch is at the off position in the power on condition. After the mechanism is set into the stop condition, and the camera zoom lens is moved to the wide end, the VTR on is made low. While the power supply battery is loaded, the unit waits while scanning the power key input. However, if the battery (or AC adapter) is removed, and the $\overline{\text{BATTERY OFF}}$ becomes low, it is set into the sleep mode. The oscillations of the main clock stop and the clock for clock is switched on. The power is supplied from the lithium battery, and only the clock operates until the battery is loaded once again.

6-6-3. Power Processing by STAND-BY Switch

When the power switch is at the camera side, power on/off operations by the STAND-BY switch can be performed.
Following, even if the power switch is at the camera side, power on processing will not be performed if the STAND-BY switch is at the READY side. Moreover, even if the power switch is at the camera side, power off processing will be performed if the STAND-BY switch is at the HOLD side.
The zoom lens of the camera will not move to the wide end for power off by STAND-BY switch operations.
Refer to the "Instruction Manual" for details on operation methods.

6-7. MECHANISM CONTROL

The control of mechanisms includes cassette tape loading and unloading, capstan motor tape travel speed control and ON/OFF control and direction control, and drum motor ON/OFF.
Precise rotation control of the capstan motor and drum motor is performed by the independent servo-control program in the main controller.
Details are described in the following chapter.
During mechanism operations, check the various sensors. If faults are detected, perform the avoidance operation described in the following section.
For details on mechanism operations, refer to the chapter on mechanism.

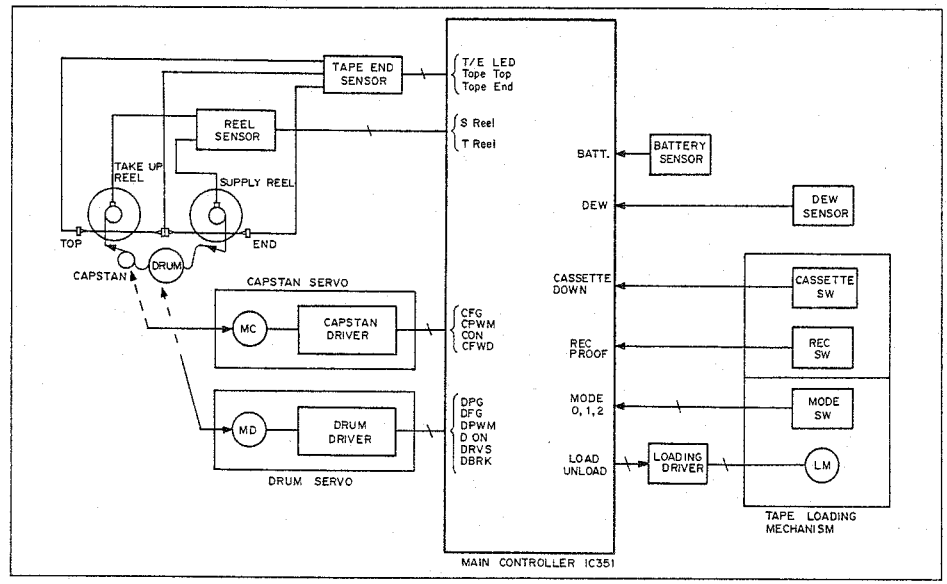


Fig. 6-7. Mechanism control circuit

6-7-1. Tape Loading Control Circuit

The drive circuit of the loading motor is shown below.
ON/OFF operations and the rotary direction are controlled by the LOAD and UNLOAD signals.
A power (5V) is supplied from the fixed voltage power by the voltage regulator circuits (IC341, Q3401).

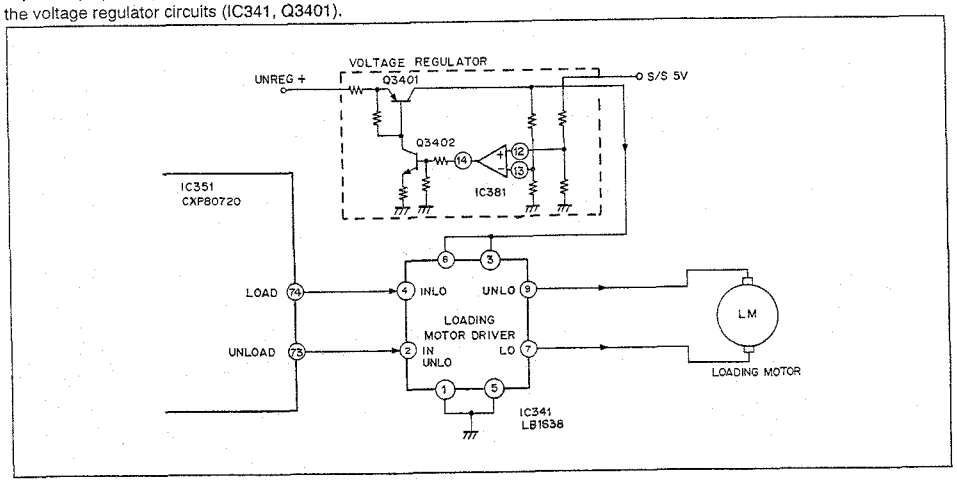


Fig. 6-8. Roading Control Circuit

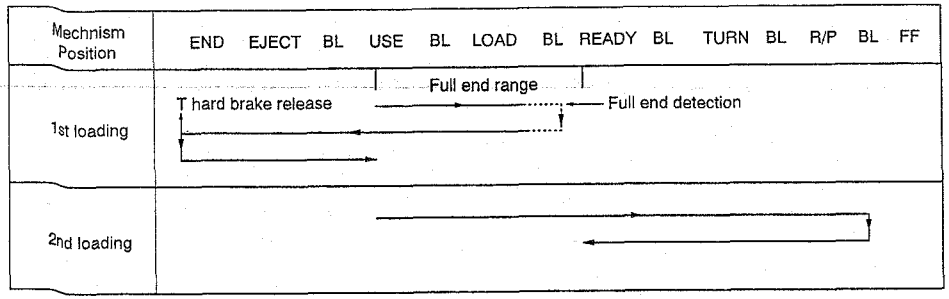
A mode detecting switch is equipped to detect the position of the mechanism during tape loading and unloading. This switch shows the relation between the mode switch and the mechanism.
For further details, refer to Mechanism Service Technical Information "A Mechanism".

MECHANISM POSITION	MODE SW			MECHANISM CONDITION	MECHANISM OPERATION
	2	1	0		
END	1	1	0	Used during full end processing	T side hard brake release
EJECT	1	0	0		Cassette holder up operation
BL	1	1	1		
USE	1	0	1	Cassette in stand-by	
BL	1	1	1		Loading operation Unloading operation
LOAD	1	0	0		
BL	1	1	1		
READY	0	0	1	Pinch roller press release	Pinch roller OFF Tension regulator OFF
BL	1	1	1		
TURN	0	1	1	Tape running possible (Pinch roller release)	Pinch roller OFF Tension regulator ON
BL	1	1	1		
R/P	0	1	0	Tape running possible (Pinch roller press)	Pinch roller ON Tension regulator ON
BL	1	1	1		
FF	0	0	0	Tape running possible (Pinch roller press)	Pinch roller ON Tension regulator half ON

Table 6-4 Mode switch and mechanism condition

6-7-2. Full End Loading Processing

This mechanism adopts the SS loading format. Tapes which have reached full end in other units will not reach loading end when loaded in this unit.
In this case, if the tape end is detected during LOADING, the tape returns in the unloading direction, and moves to the end position which it normally will not move to. After the T hard brake is released, the cassette compartment will move up once. If loading is performed after this again, as the T hard brake has been released, the tape is also pulled out from side T and is able to move to the loading end.


Mechnism Position
END EJECT BL USE BL LOAD BL READY BL TURN BL R/P BL FF
Full end range
T hard brake release
Full end detection
1st loading
2nd loading

6-7-3. Tape Feeding When Continuous Shooting

When the recording mode is changed to the PAUSE mode using the START/STOP keys, the tape is rewound to a certain extent
(REC_PAUSE_REVERSE), then forwarded slightly (REC_PAUSE_FORWARD_1), and stopped. When the record mode is set the next time, tracking is adjusted to the previously recorded pattern (REC_PAUSE_FORWARD_2) before recording begins.
In this way, the video and pilot signals are controlled so that they continue in sequence on the tape and prevent the playback image from being disrupted at the joint points of continuous shooting.
The amount of tape travel is controlled by measuring the number of pulses CFG from the capstan motor. Over-writing is carried out for 14 tracks to prevent non-recorded sections from being produced at the tape parts shot continuously.

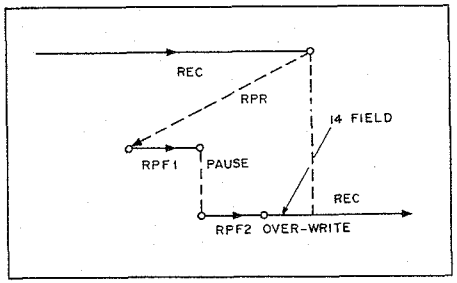


Fig. 6-9. Continuous shooting control

	Capstan Speed	Field No.		
		NTSC	PAL	
			SP	LP
RPR	−×3 Speed	124	100	152
RPF 1	×1 Speed	76	52	104
RPF 2	×1 Speed	34	34	30
Over-writing	×1 Speed	14	14	18

Table 6-5

6-8. AVOIDANCE OPERATION AND POWER SAVING MODE DURING FAULTY OPERATIONS

In some cases, it may not be possible to continue the normal operation mode due to the condition of the deck.
The deck is equipped with various detecting elements to detect these conditions. A warning produced by the detecting signal is displayed on the screen, and if necessary, the deck is made to automatically shift into the safe waiting mode.
Refer to section 6-11 in the latter part of this manual for the types of warning display.
Moreover to prevent tape and mechanism friction, if the PAUSE and STILL modes continue for 5 minutes, the deck will automatically shift into the following modes.
PAUSE → POWER OFF
STILL → STOP

Error code are set in accordance with the various types of system faults so that the causes of faults which have developed can be analyzed more easily.
When a fault has developed, the error code will be displayed by pressing the STOP and PAUSE keys at the same time for two seconds continuously.

Error codes are given below.

Error Code	System Alarm Status
E01 E04	T. REEL rotation stop during tape FWD travel S. REEL rotation stop during tape RVS travel
E11	Loading direction mechanism position detection fault (Including loading motor stop)
E12	Unloading direction mechanism position detection fault (Including loading motor stop)
E21	Drum motor rotation fault (stop, disruption, etc.)
E22	Drum motor start failure
E23	Capstan motor rotation fault (stop, disruption, etc.)
E24	Capstan motor start failure

Table 6-6. Error codes

The following is an outline of the circuit operations of the various detecting elements for fault detection.

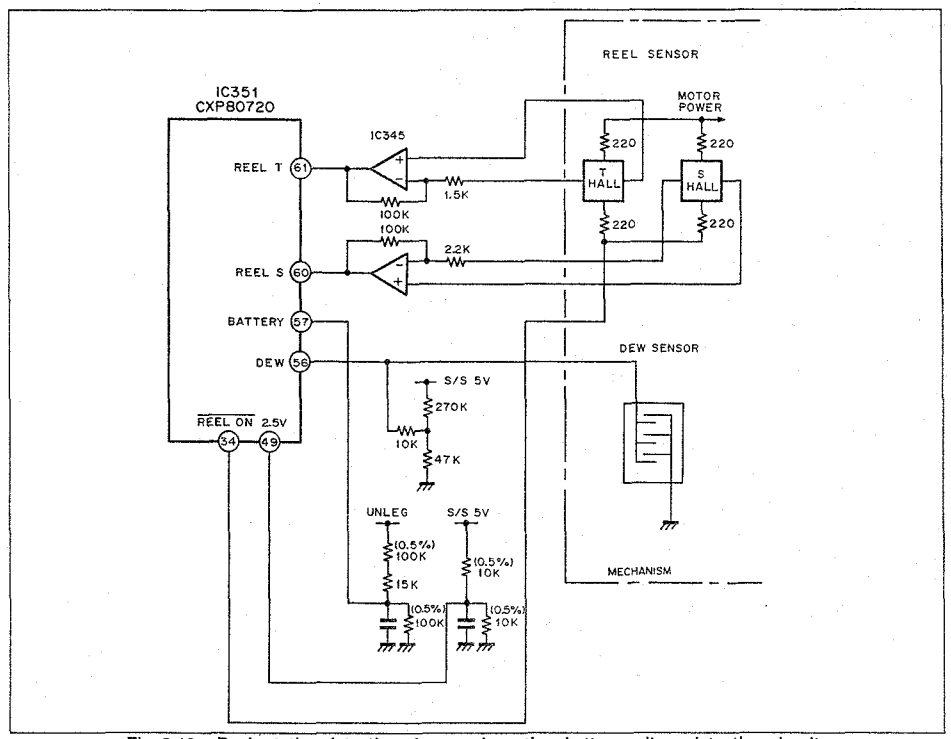


Fig. 6-10. Reel rotation detection, dew condensation, battery voltage detection circuits

6-8-1. Reel Rotation Check

Reel rotation is detected by the pulse from the hall device mounted on the reel base of the take-up side and supply side.

As the signal from the hall device is very small, it is amplified by IC345, and then input to the analog input terminal of the main controller (Pin ㊿ of supply side/Pin ㊶ of take-up side).

The level of the signal at every T1 msec. and cycle T2 are measured in the main controller as shown in the figure below. Moreover the signal center level required for measuring T2 is also measured at every cycle.

When the reel pulse cannot be detected even if the capstan motor is rotated, the reel rotation is judged to have stopped. The capstan motor rotation is stopped, and the tape take-up processing is performed. The mechanism is then moved to the READY position.

If the pulse is not input during the following period, the unit is judged to have stopped.

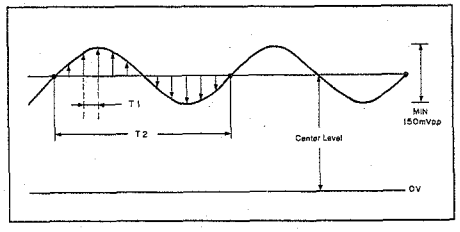


Fig. 6-11. Reel rotation detection timing

Mode	Detection time T1	Stop determination time
FF, REW, FR-SEARCH	6 msec.	0.8 sec.
CUR, REV	18 msec.	1.0 sec.
Other than above	100 msec.	3.0 sec.

Table 6-7. Reel detection time and stop determination time

6-8-2. Dew Check

The dew sensor is normally set to a low value of below 20 k Ω but becomes a high value of 120 k Ω when there is dew.

The resistance value of the dew sensor is detected by the analog input terminal of the main controller (Pin ㊻). Dew is determined when the value is above 0.43 V.

When there is dew, the drum motor is stopped, and the mechanism is set into the READY condition.

Keys other than POWER and EJECT will not work.

Once dew has occurred, it will take approximately 1 hour to clear the problem.

6-8-3. Battery Voltage Check

To detect the battery voltage, the voltage obtained from dividing the UNREG voltage by the resistance (BATTERY) and the voltage obtained from dividing the S/S5V voltage by the resistance (2.5V) are input to the analog input terminal (2.5V:Pin ㊾ /BATTERY: Pin ㊼) of the main controller.

The value of this voltage is read, and the processing for voltage drop is performed.

The threshold voltage used for this processing is set as follows:

Pre-end voltage: Approx. 5.55V

End voltage: Approx. 5.45V

When the battery pre-end is detected, a warning is displayed on the viewfinder. When the the voltage of the battery drops and battery end is detected, the power supply is turned off. (The time taken from pre-end to end detection is approximately 1 to 5 minutes.)

6-8-4. Tape End/Top Check

The center of the cassette table is equipped with the LED emitting element to detect the top and end of the tape.

Both ends of the cassette base are also equipped with two photo sensors each. By checking which photo sensor receives the light traveling through the transparent section of the tape end/top section from the LED, the end section can be determined. When both receive the light, tape absence is determined. Light emission is in pulse form, and sync detection is performed. Refer to the figure.

The signals from the photo sensors on both sides are input to the analog input terminal of IC351.

(Pin ㊺ of tape end side/Pin ㊶ of tape top side)

In the main controller, the output level difference between before the tape LED lights and after is checked. If the difference is above 0.7 V, tape end or tape top is determined.

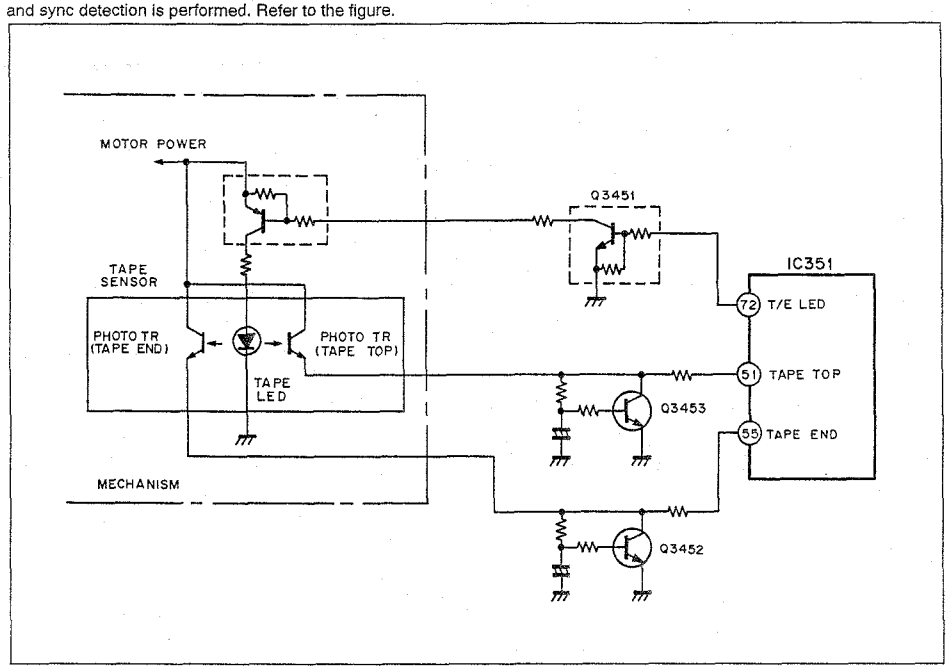


Fig. 6-12. Tape Top/end detection circuit

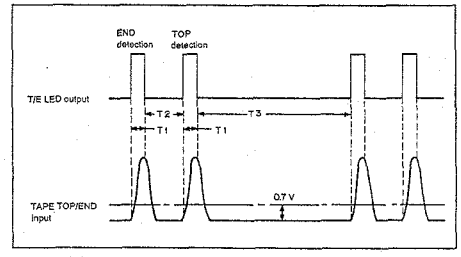


Fig. 6-13. Tape top/end detecting timing

Mode	T1 (Lit)	T2 (Turns off)	T3 (Turns off)
FF, REW, FR-SEARCH	1 msec.	3 msec.	3 msec.
CUR, REV	1 msec.	3 msec.	5 msec.
Other than above	1 msec.	3 msec.	95 msec.

Table 6-8. Tape top /end detection time

6-8-5. Drum Motor Rotation Check

Rotation errors are checked in the main controller by the drum motor rotation pulse (DFG) used for the servo.
If the rotation pulse is not detected even after 3 seconds have passed since drum motor start up, the mechanism is set to READY. This is also set when rotation speed during normal operations is shifted by more than ± 30%.
Keys other than POWER and EJECT will not work.

6-8-6. Capstan Motor Rotation Check

When the capstan motor rotation pulse (CFG) has not been input for more than 3 seconds, READY is set, and keys other than POWER and EJECT will not work.

6-9. ADJUSTING MODE

The adjusting mode can be selected by shortening Pin ⑫ (GND) and Pin ⑬ (TEST) of J1005 on the CP1 board with a lead wire.
The following alarm sensing functions and power saving avoidance mode transfer functions are not made in the adjusting mode.

1. Reel rotation sensing.
2. Dew sensing.
3. Drum faulty rotation sensing.
4. Power OFF due to battery down.
5. Mechanism protection function

For further details on adjustments, refer to the Service Manual.

6-10. CONTROLLER IC TERMINAL SPECIFICATIONS

The functions of the input/output signals of the microprocessor used in the system control circuit and the characteristics of the signal logic are listed in the table in accordance with the terminal number.

6-10-1. Main-controller

CXP80720(IC351)
1 chip microprocessor
ROM capacity: 20 Kbytes×8 bits
RAM capacity: 800 bytes×8 bits
Package:QFP Pin 100

Pin	Signal Name	I/O	Outline
1	REC H	O	High output during REC mode
2	JOG. H	O	High output during special playback mode
3	$\overline{\text{ON SCREEN}}$	O	On screen display control signal
4	V.MUTE	O	Video circuit mute signal, H: Mute
5	SP/$\overline{\text{LP}}$ OUT	O	SP/LP mode discrimination signal
6	$\overline{\text{REMOCON ON}}$	O	Remote controller photo sensor power supply control signal
7	$\overline{\text{CG VD}}$	O	Sync signal for on screen display IC
8	DRUM BRK	O	Drum motor brake signal, H: Brake ON
9	CG.STB	O	On screen display IC chip select signal
10	VTR ON	O	VTR section DC/DC converter control signal
11	CAM ON	O	Camera section DC/DC converter control signal
12	LANC CS	O	Rank control microprocessor chip select signal
13	$\overline{\text{CAMERA CS}}$	O	Camera IC chip select signal
14	NC	O	
15	CAM PW SW	I	Power supply switch input signal (Camera)
16	VTR PW SW	I	Power supply switch input signal (VTR)
17	EJECT SW	I	EJECT switch input signal
18	S/S SW	I	S/S switch input signal
19	STNBY SW	I	STNBY switch input signal
20	$\overline{\text{TEST}}$	I	Adjustment mode discrimination signal, L: Adjustment mode
21	REMOTE SAN/$\overline{\text{TCE}}$	I	Remote controller specifications, Discrimination signal
22	SCAN OUT	O	Input extension matrix output signal
23	$\overline{\text{SCAN IN 0}}$	I	Input extension matrix input signal
24	$\overline{\text{SCAN IN 1}}$	I	Input extension matrix input signal
25	$\overline{\text{SCAN IN 2}}$	I	Input extension matrix input signal
26	$\overline{\text{SCAN IN 3}}$	I	Input extension matrix input signal
27	$\overline{\text{AUTO SW}}$	I	Auto lock switch input signal
28	MODE SW 2	I	Loading position detection signal
29	MODE SW 1	I	Loading position detection signal
30	MODE SW 0	I	Loading position detection signal
31	$\overline{\text{SCAN OUT 0}}$	O	Input extension matrix output signal
32	$\overline{\text{SCAN OUT 1}}$	O	Input extension matrix output signal
33	A.MUTE	O	Audio circuit mute signal, H: Mute
34	$\overline{\text{REEL ON}}$	O	Reel pulse on/off control signal
35	$\overline{\text{PB}}$	O	Playback image/EE image switching signal, L: Playback image
36	STBY	O	Video circuit power supply on/off control signal
37	$\overline{\text{TALLY LED}}$	O	TALLY LED on/off switching signal
38	$\overline{\text{VIDEO CS}}$	O	VIDEO IC chip select signal
39	MP		
40	$\overline{\text{RESET}}$	I	Microprocessor reset signal input
41	VSS		
42	XTAL		Main clock oscillation circuit
43	EXTAL		Main clock oscillation circuit
44	$\overline{\text{CSO}}$		

Table 6-9. CXP80720 Terminal Specification

Pin	Signal Name	I/O	Outline
45	SIN	I	Main microprocessor serial data input
46	SOUT	O	Main microprocessor serial data output
47	$\overline{SCK}$		Main microprocessor serial clock input/output
48	T/E LEBEL	AN11	T/E sensor threshold level value, normally level L
49	2.5V	AN10	Battery down determination standard signal
50	AD SW	AN9	AD switch input level discrimination signal
51	TAPE.TOP	AN8	Tape top sensor detection input
52	AVSS		A/D conversion GND
53	AVREF		Maximum voltage of A/D conversion
54	AVDD		A/D conversion VDD
55	TAPE.END	AN7	Tape end sensor detection input
56	DEW	AN6	DEW sensor detection input
57	BATTERY	AN5	Battery voltage detection input
58	V.CENTER	AN4	Video center adjustment input
59	LP.STILL	AN3	+Steel noise absorbing adjustment input during LP mode
60	REEL S	AN2	Supply reel rotation detection input
61	REEL T	AN1	Take up reel rotation detection input
62	ATF ERROR	AN0	ATF error signal input
63	$\overline{NTSC}$/PAL	I	NTSC/PAL discrimination signal, H: PAL
64	DPG	I	Drum PG input
65	LANC Y/$\overline{N}$	I	LANC Present/Absent H:Present
66	C.SYNC	I	Composite sync input
67	REC PROOF	I	Cassette recognition SW signal, H:Record prohibition
68	DPG	I	Drum PG input
69	DFG	I	Drum FG input
70	CFG	I	Capstan FG input
71	NC		
72	TE.LED	O	Tape end sensor LED on/off signal
73	UNLOAD	O	Loading motor control signal, H: UNLOAD
74	LOAD	O	Loading motor control signal, H: LOAD
75	CAP.PWM	O	Capstan servo PWM signal
76	DRUM.PWM	O	Drum servo PWM signal
77	ATF.LOCK	I	SP/LP automatic discrimination signal input
78	$\overline{CST\ DOWN}$	I	Cassette holder up/down detection input
79	CAP F/$\overline{R}$	O	Capstan motor forward/reversal control signal
80	DRUM $\overline{F}$/R	O	Drum motor forward/reversal control signal
81	DRUM ON	O	Drum motor on/off control signal
82	$\overline{BATTERY.\ OFF}$	I	Battery down detection input (4.3V)
83	NU(16kHz)		
84	CAP ON	O	Capstan motor on/off control signal
85	REMOTE	I	Infrared remote controller signal input
86	TEX		Clock (32.768 KHz) oscillation circuit
87	TX		Clock (32.768 KHz) oscillation circuit
88	VSS		VSS of CPU digital section

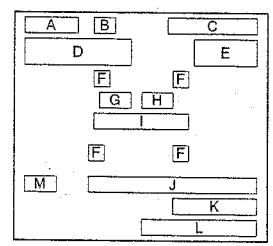
Table 6-9. CXP80720 Terminal Specification

Pin	Signal Name	I/O	Outline
89	VDD		VDD of CPU digital section
90	NC		
91	JOGVD	O	Quasi sync signal for video
92	$\overline{FEP}$	O	Flying erase head switching signal
93	$\overline{REC\ CH\ A}$	O	CHA recording control signal
94	$\overline{REC\ CH\ B}$	O	CHB recording control signal
95	RF SW	O	Head switching signal
96	P46 16	O	46 kHz/16 kHz switching signal of pilot signal
97	SEL 2	O	Pilot sequence control signal
98	SEL 1	O	Pilot sequence control signal
99	TSB	O	SP/LP automatic discrimination gate pulse
100	$\overline{POWER\ SAVE}$	O	Video ATF circuit mode switching signal, H: Playback

Table 6-9. CXP80720 Terminal Specification

6-11. SCREEN DISPLAY SPECIFICATION

The various status characters displayed in the viewfinder in the deck and on the screen of the external TV are summarized in the following.



A: Operation mode
B: Tape speed
C: Counter
D: Preset mode/Operation mode (2×2 double angle)
E: Focus (2×2 double angle)
F: Sports mode frame
G: Battery warning
H: Cassette warning
I: Warning (Tape end, dew)
J: Battery adjustment
K: Time
L: Date
M: System error code

Fig. 6-14. Character display positions on screen

Display Position/Contents			Diisplay Character in VF		Mode
A	Operation mode	a REC b PAUSE c STOP d PALY e FF f REW	REC PAUSE STOP PLAY FF REW	Lit Blinking Lit Lit Lit Lit	REC mode PAUSE mode STOP mode (only VTR) PLAY mode FF mode REW mode
B	Tape speed	a SP b LP	SP LP		All modes
C	Counter	a Linear time counter	M-1:15:37	Lit	All modes
D	Preset mode/ Operation mode	a Sports b Auto high-speed shutter c Close up d Low light e Flickerless		Lit	CAMERA PW ON E-E
	Mode display	f REC g PAUSE	REC PAUSE	Lit Blinking	CAMERA PW ON E-E
E	Auto-focus	a Automatic b Manual c Manual d Manual	AF MF MF+ MF –	Lit	CAMERA PW ON E-E
F	Sports mode frame	a Central emphasis AF		Lit	CAMERA PW ON E-E
G	Battery warning	a Battery voltage decrease		Blinking	During voltage decrease detection
H	Cassette warning	a Recording not possible b No cassette c System error detection		Blinking Blinking Fast blinking	
I	Warning (Tape end, dew)	a Dew condition b Tape remainder below 5 min. c Tape end	TAPE TAPE END	Blinking	REC mode
J	Battery voltage drop adjustment		≫‖≪BATT		Adjustment mode
K	Time display	b Time	14:25:48		CAMERA PW ON E-E
L	Date display	a Date	21.10.1992		CAMERA PW ON E-E
M	Error code	a Error code	E04	Lit	During system error detection

Table 6-10. Display specifications

7. SERVO SYSTEM

7-1. OUTLINE

In the VTR, rotation of the drum motor and capstan motor is controlled by the servo circuit.

- In the recording mode, the video signals must be recorded on the tape at the proper pitch.
  The drum servo controls rotation of the drum motor so that the rotational phase of the drum motor is always synchronized with the phase of the video signal to be recorded. Thus the vertical sync signal of the video signal is recorded on the specified tape position.
  The rotation of the capstan motor is controlled for a constant speed. Therefore the tape speed become constant and the signals are recorded on tape at the proper pitch.

- In the playback mode, the servo control the both motors to obtain the maximum playback signal with no time base fluctuations.
  The rotation of the drum motor is controlled for a constant speed.
  In 8mm video, a system called ATF is adopted so as to control the rotation of the capstan motor for optimum tracking over the recorded tracks.

7-2. CONFIGURATION

The overall block diagram for the servo system is shown in Fig. 7-1.
The servo system can basically be divided into the following blocks:

a) Rotation Detection Element and Amplifier
   The motor is equipped with a detection element for rotation detection. The very low level signal obtained from the element is amplified to a logic level by the amplifier, and input to the servo processing circuit.

b) Servo signal processor block
   This block detects the rotational speed and phase of the motor based on the sensor signal and processes the resulting detection signal. The signal processing is performed by the microprocessor.

c) Power amplifier, motor driver and motor
   The control signal is converted into a power signal for driving the motor.

d) ATF signal processor block
   In order to get optimum tracking, in 8mm video, a signal called pilot signal is recorded on tape in the recording mode and the ATF error signal corresponding to the shift amount of the tape running is detected by the recorded pilot signal in the playback mode.

The circuit is configured almost entirely from ICs. The ICs, etc., which comprise the various blocks are shown in Table 7-1.

	Drum System	Capstan System
Rotation sensor	Print coil type sensor (PG/FG)	MR sensor
Sensor amplifier	BA14741F	Bilt-in Mechanism
ATF detection	– – –	LV4050W
Speed/phase detection **Servo signal processing**	CXP80720	
Motor driver	CXA8006MQ	Bilt-in Mechanism
Motor	Three-phase bi-directional sensorless motor	Hall element detection type brushless motor

Table. 7-1.

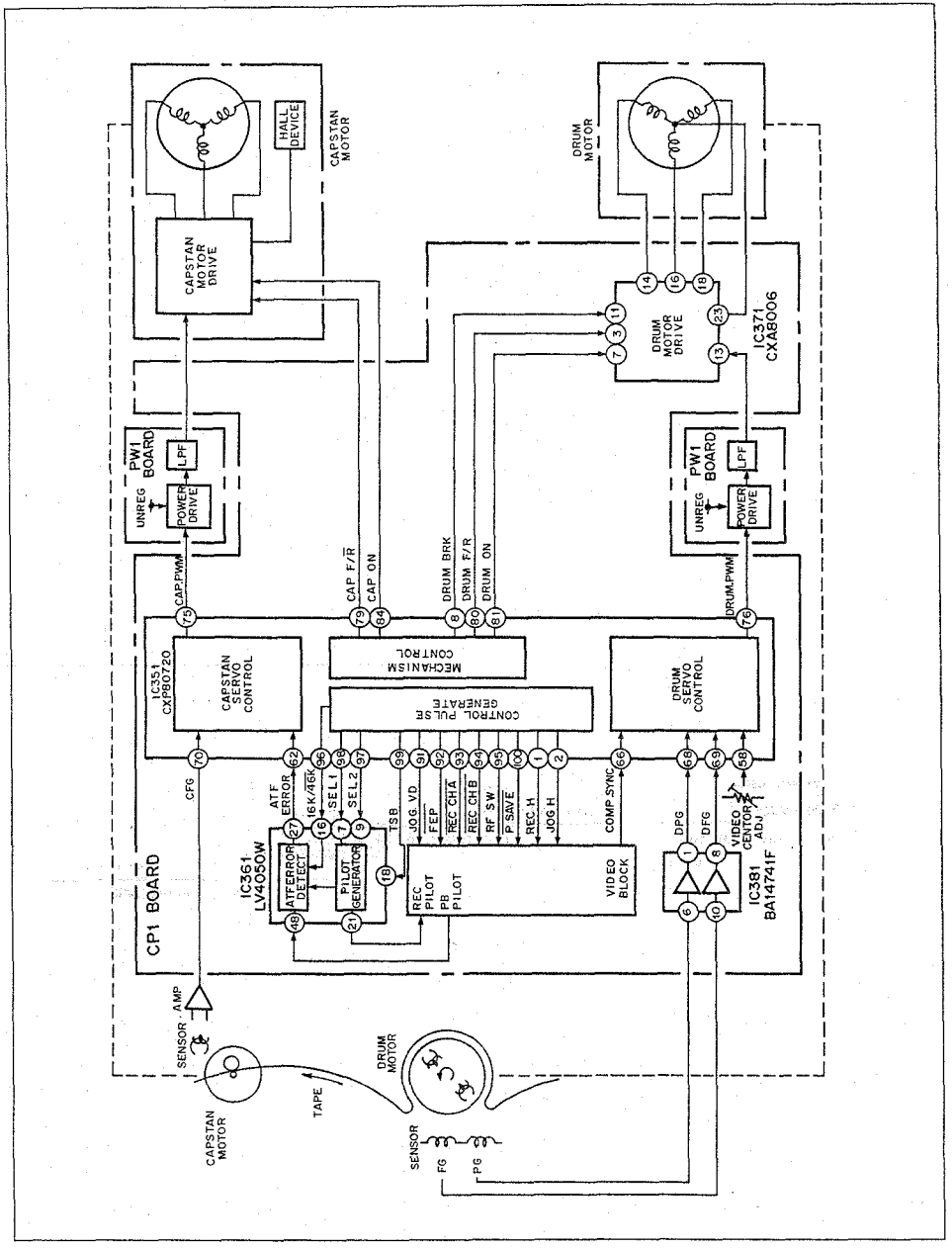


Fig. 7-1.

7-3. DRUM SERVO SYSTEM

7-3-1. Drum Rotation Sensor and Amplifier

In order to detect the rotation, a printed coil type detection element is used to the drum motor. From the detectors, following two signals are output.

The DFG (Drum Frequency Generator) coils are mounted along the circumference of the drum at intervals of 30 degrees in the rotational angle to obtain a 12-cycle sine wave per each drum rotation.

One DPG (Drum Phase Generator) coil is mounted at the specified position along the circumference of the drum to obtain a 1-cycle pulse per each drum rotation. The DPG functions as a marker to show physical drum mounting position.

The schematic diagram for the sensor amplifier is shown in Fig. 7-2. The signals output from the sensors are input to BA14741F (IC381) where it is amplified to a logic level.

The waveforms are shown in Fig. 7-3.

As the drum motor rotates at 25 rps during normal operation, the frequencies are as follows:

DPG=25 Hz

DFG=12×25=300 Hz

The DPG (Pin ⑥ input/Pin ① output) is amplified by BA14741F (IC381) are input to Pins ⑭ and ⑯ of CXP80720 (IC351).

The DFG (Pin ⑩ input/Pin ⑧ output) is input to Pin ⑯ of CXP80720 (IC351).

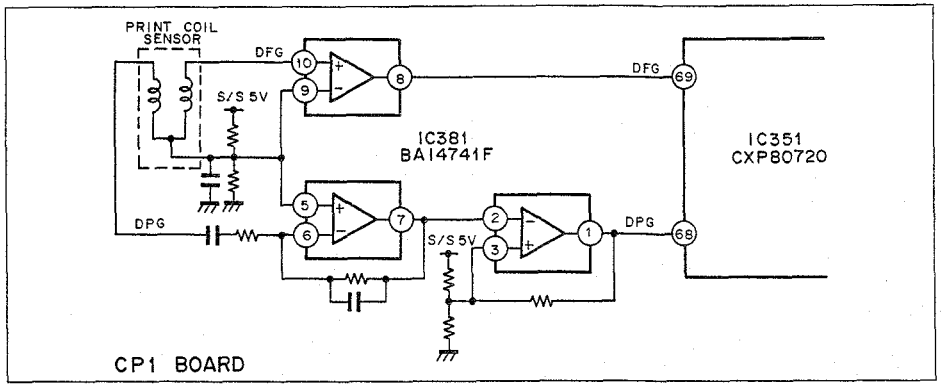
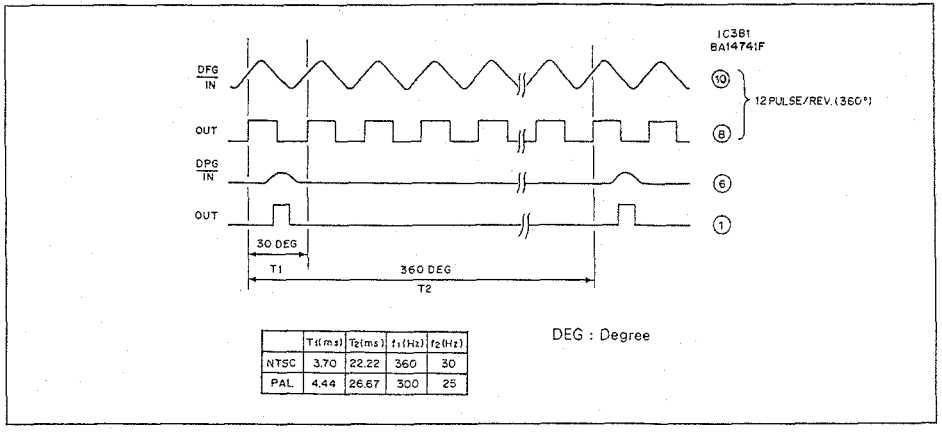


Fig. 7-2. Sensor amplifier circuit



	T1(ms)	T2(ms)	f1(Hz)	f2(Hz)
NTSC	3.70	22.22	360	30
PAL	4.44	26.67	300	25

Fig. 7-3. DFG and DPG signals

7-3-2. Speed/phase Detection and Servo Data Signal Generation

The rotational speed and phase of the drum motor is detected by the pulses output from the DPG and the DFG. Detection is performed by the microprocessor CXP80720 (IC351).
The processing is shown in Fig. 7-4.
The DFG is divided synchronizing with the phase of the DPG.

[Speed Detection]
Speed detection is performed by measuring the period of DFG signal, which is input to Pin ⑲ of CXP80720 (IC351). Speed detection is carried out at every 30 degrees of the rotational angle.

[Phase Detection]
In the recording mode, the rotational signal phase must be synchronized with the phase of the video signal to be recorded.
The drum rotational phase is synchronized with the vertical sync pulse which is separated within CXP80720 (IC351) from the composite sync signal input to pin ⑯ of CXP80720 (IC351).

[Servo Signal Generation]
The servo data is generated by processing the phase and speed detection data. The generated data is converted within the CXP80720 (IC351) into the PWM signal and output from Pin ⑯ as DRUM.PWM signal.

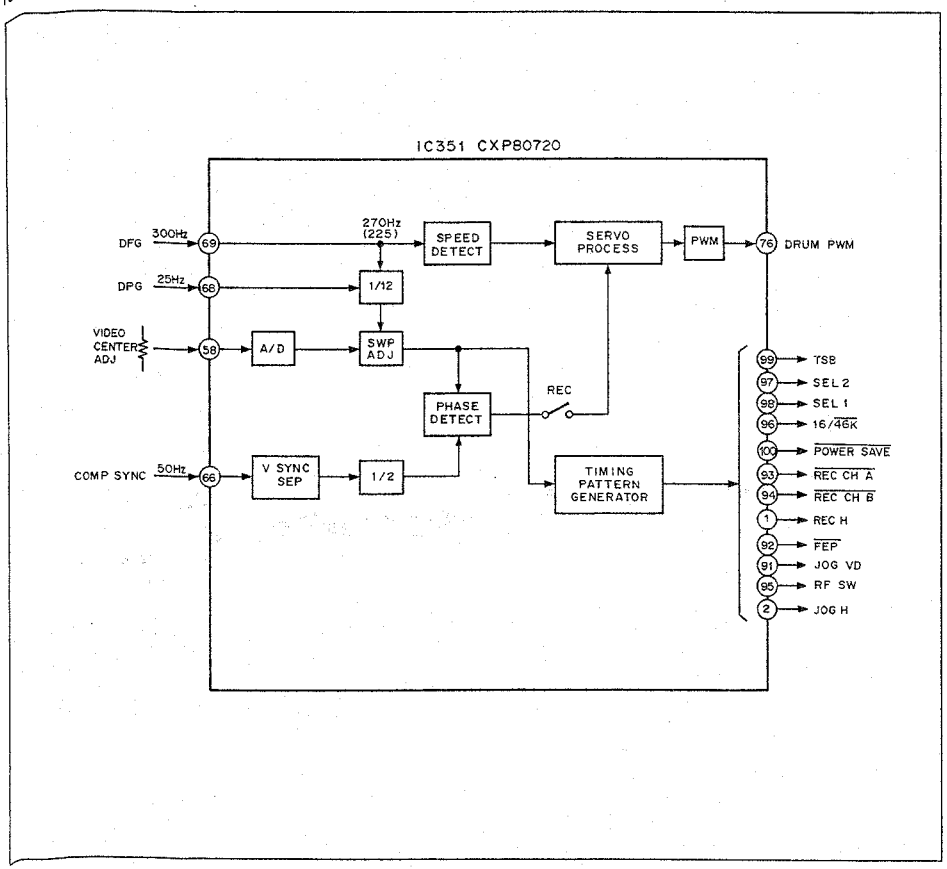


Fig. 7-4. Drum servo processing

7-3-3. Power Amplifier, Motor Driver and Motor

A 3-phase 8-pole brushless motor is used as drum motor. IC371 (CXA8006) is used for the motor drive.
Fig. 7-5 shows the drum motor driver circuit.
The PWM signal (DRUM. PWM, 46.8kHz) output from CXP80720 (IC351) is passed through the power amplifier Q3003 and converted to a DC voltage with filters composed of L3003 and C3004 and then input to Pin ⑬ of IC371 as a supply voltage Vs for motor driver.
The amplitude of the driving waveforms (output of Pins ⑱, ⑯ and ⑭) for the U, V and W phase coils are determined by the voltage of Vs.
The rotate/stop control signal (DRUM ON) from the main controller (Pin ⑯ of IC351(CXP80720)) is input to Pin ⑦ of IC371. The motor rotates at high level.
In Low, the whole IC takes standby mode. Motor's reverse control signals (DRUM F/R) are input to Pin ③ on IC383 (CXA8006). In mode changing, when rotation's speed is reduced suddenly, the instruction code will be sent from Pin ⑩ on IC351 (CXP80720).

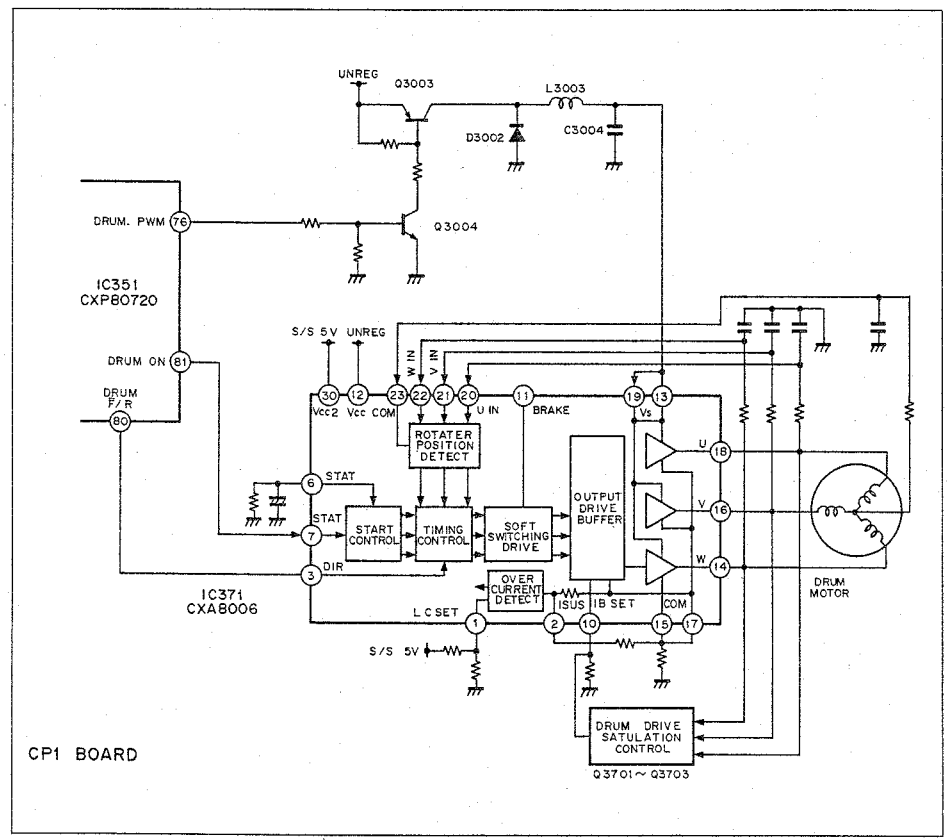


Fig. 7-5. Drum motor driver circuit

7-4. HEAD SWITCHING SIGNAL RFSW CREATION

This unit adopts a 2 heads structure cylinder drum as shown in Fig. 7-6. Both heads alternately record and play back the tape pattern of 1 track. 1 track corresponds to 180 degrees of the rotational angle of the drum.

The RFSW signal is generated as a switching signal for selecting the recording/playback head. The switching timing of the RFSW signal is generated with the DFG as a reference. The DPG pulse is used to identify the pulse corresponding to the head installing position from amongst the 12 pulses of one rotation. The timing chart of processing is shown in Fig. 7-7.

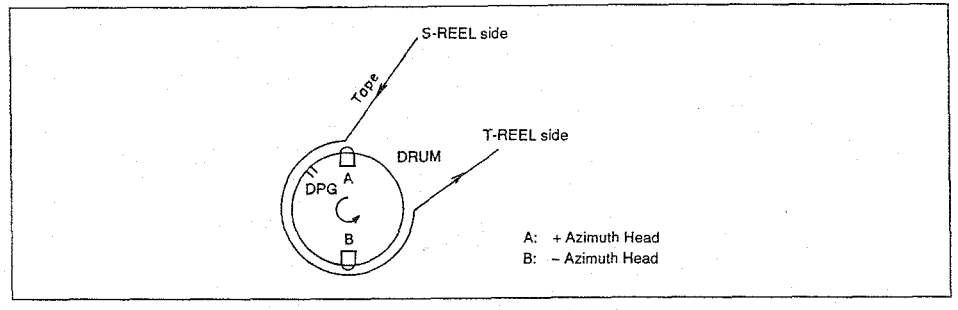


Fig. 7-6. Drum and head configuration

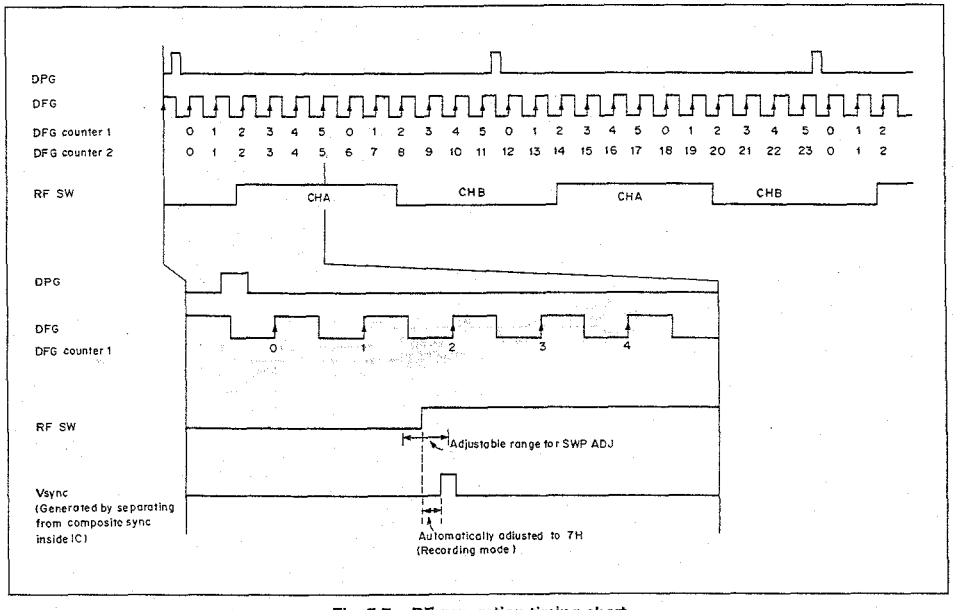


Fig. 7-7. RF generation timing chart

7-4-1. Switching Point Adjustment

The signal recording position on the tape is determined by the switching timing of the RFSW signal. There is a variable delay circuit for correcting the deviation of the switching timing due to variations of the DFG mounting position.

The RFSW signal switching timing can be adjusted by the voltage at the Analog input Pin ㊽ (SWP ADJ) of CXP80720. Switching point is adjusted by playing back a properly recorded alignment tape and by setting the RFSW timing.

7-4-2. Video Signal Recording Phase (7H) Setting

The vertical sync signal of the video signal will be recorded on the tape at the specified position conforming to a format. In the recording mode, the time difference between the RFSW signal switching point and the vertical sync signal is automatically set to 7H (448 µsec) by the servo system. Therefore, the deck which has been properly adjusted the switching point, allows to record the video signals on the tape at the proper format.

7-4-3. Timing Control Signal

In addition to the RFSW signal, various signals for controlling the video and audio circuits are generated by CXP80720 (IC351).

Fig. 7-8 shows the waveforms of these control signals.

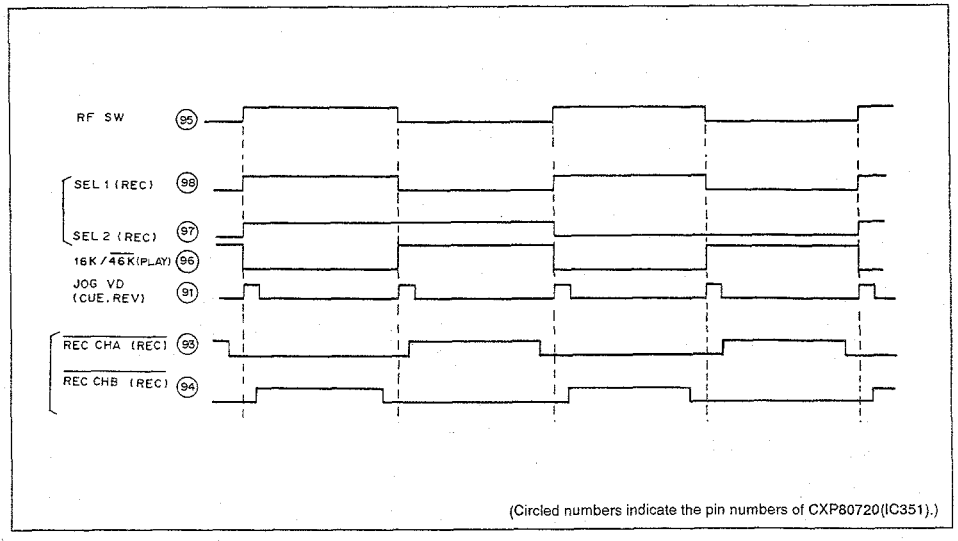

RF SW (95)
SEL 1 (REC) (98)
SEL 2 (REC) (97)
16K/46K(PLAY) (96)
JOG VD (CUE, REV) (91)
REC CHA (REC) (93)
REC CHB (REC) (94)
(Circled numbers indicate the pin numbers of CXP80720(IC351).)

Fig. 7-8. Video ATF control signal

7-5. CAPSTAN SERVO SYSTEM

7-5-1. Sensor and Sensor Amplifier

The MR sensor (magnetic resistance sensor) is used as rotation detection sensors for the capstan motor. This allows for a 520-cycle waveform per one rotation.

The sensor output signal CFG is amplified to the logic level by amplifer in the mechanism, and is input to Pin ⑦⓪ of CXP80720 (IC351).

In the recording mode, the motor rotates at approximately 2.670 rps in order to obtain a tape speed of 20.051 mm/s (SP mode). The CFG frequency is 520×2.670=1388Hz at this time.

7-5-2. Speed/Phase Detection and Servo Signal Processing

In the same manner as the drum servo, detection of the phase and speed and the processing of the servo signal are carried out by CXP80720(IC351).

Fig. 7-9 shows a processing inside the IC.

The CFG input to Pin ⑦⓪ of CXP80720 (IC351) is subjected to the speed detection after division to 1/n.

(The division ratio is n=1 for normal playback.)

Either the speed control in the recording mode or the tracking control in the playback mode is made based on the speed data. The processed servo data is output from Pin ⑦⑤ as the PWM(CAP.PWM) signal.

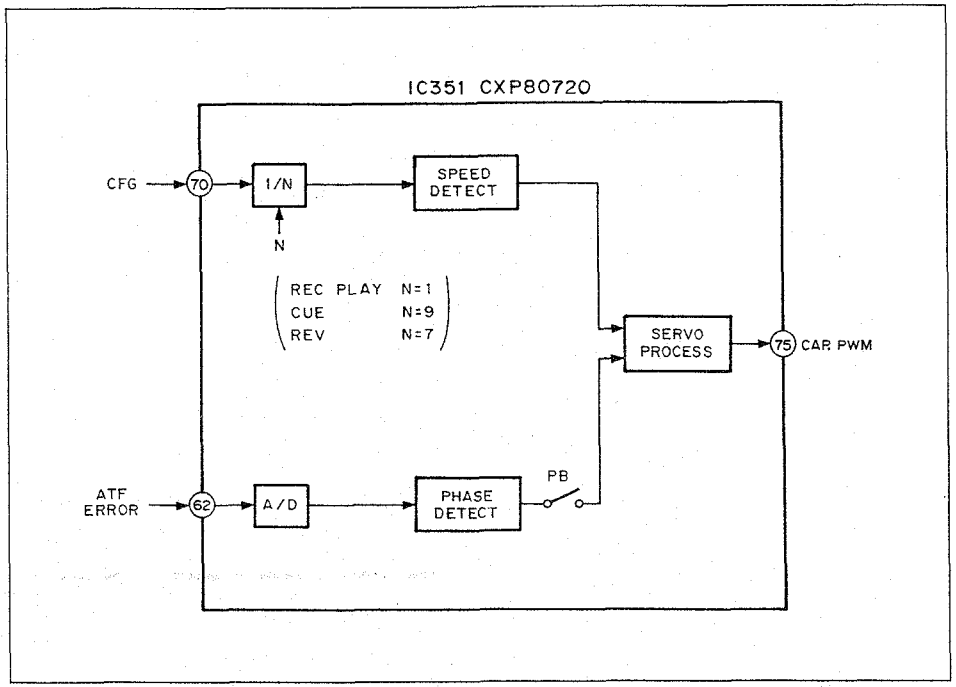


Fig. 7-9. Capstan servo processing

7-5-3. Capstan Motor and Driver

The 3-phase 8-pole hall motor is employed for the capstan motor. The motor driving circuit is built into the mechanism.

CXP80720 (IC351) outputs the rotation/stop control signal (CAP.ON: Pin ⑧④ output), rotational direction control signal (CAP.F/$\overline{R}$ Pin ⑦⑨ output) and rotational control signal (CAP.PWM: Pin ⑦⑤ output), respectively.

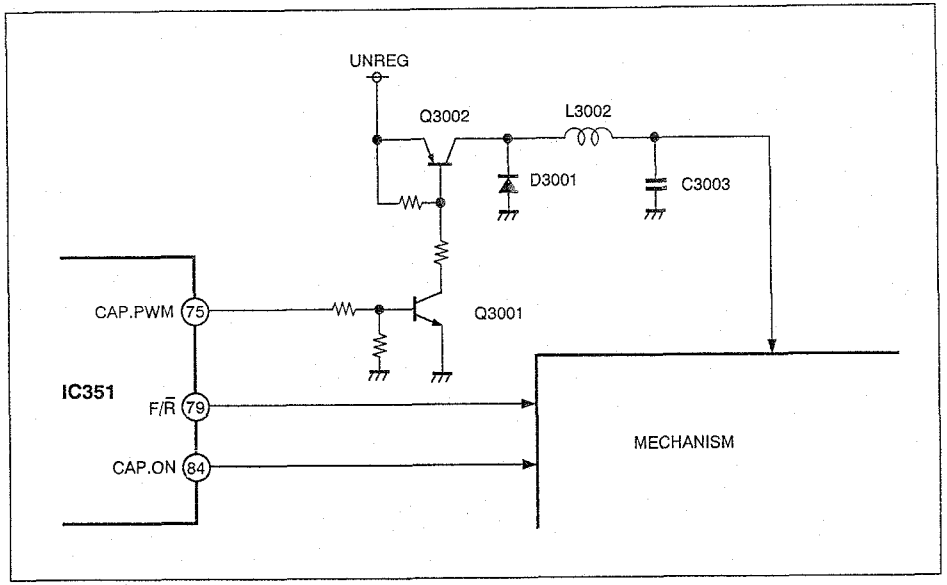


Fig. 7-10. Capstan motor driver circuit

7-6. ATF SYSTEM

In 8 mm video, an ATF (Automatic Track Finding) system is incorporated for tracking.
In this method, four types of pilot signals are recorded on the tape and these signals are processed to detect the shift amount of the trace position of the head during playback for tracking.

7-6-1. Principles

[Recording]

As shown in Fig. 7-11, the pilot signals called f1, f2, f3, and f4 overlapped on the video signal are switched for each track and recorded on the tape with the sequence repeating every 4 tracks.
The frequencies are shown in Table 7-2.
The neighboring two frequencies are selected for a mutual spectrum interval of 16/46 kHz. (See Fig. 7-12.)
f1 and f3 are recorded by + azimuth head (CHA) and f2 and f4 by – azimuth head (CHB).

Pilot (fi)	Frequency (kHz)		REC head	Frequency difference (kHz)	*N	SEL	
	NTSC	PAL				1	2
f1	102.54	101.02	CH A1		58	H	H
f2	118.95	117.19	CH B1	16	50	L	H
f3	165.21	162.76	CH A2	46	36	H	L
f4	148.69	146.48	CH B2	16	40	L	L
f1	102.54	101.02	CH A1	46	58	H	H

Table 7-2. Pilot Signal Rating

* fi =Fo/N
Fo =378 fH=5.95 MHz (NTSC) (fH=15.734 kHz)
=375 fH=5.86 MHz (PAL) (fH=15.625 kHz)

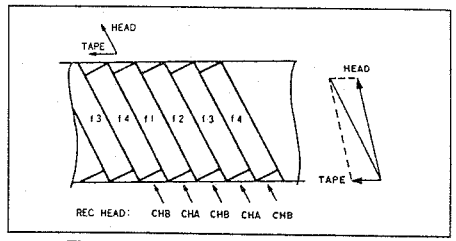


Fig. 7-11. Pilot signal recording pattern

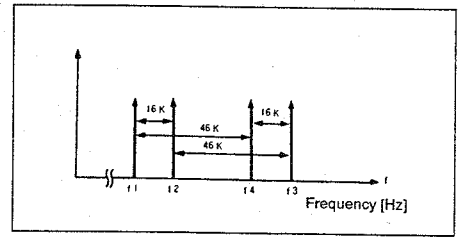


Fig. 7-12. Pilot signal recording spectrum

[Tracking Error Detection]

In the playback mode, trace position of the video head is detected by the circuit shown in Fig. 7-13.

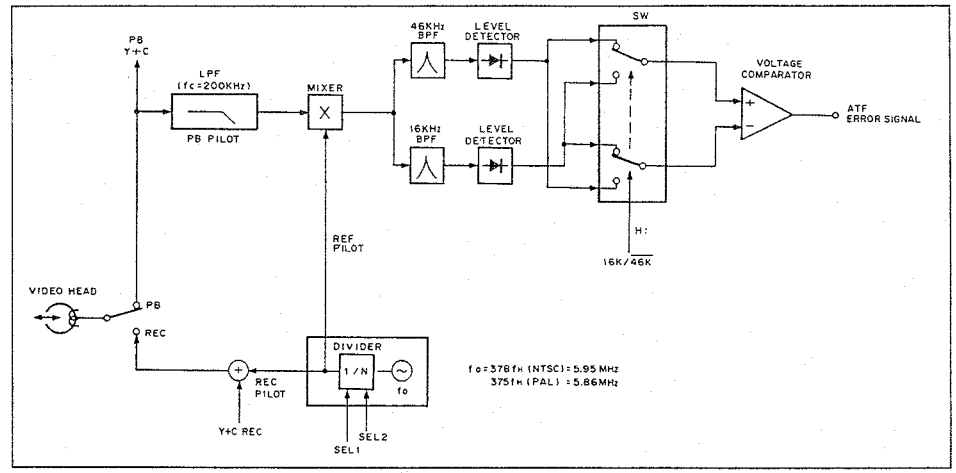


Fig. 7-13. ATF processing

A pilot signal with the same frequency as recording is used as the reference signal (REF).
Assuming that the REF is f1 and that the head is in the A position (recording f1) in Fig. 7-14.

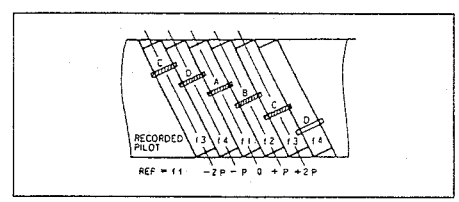


Fig. 7-14.

At this time, the playback pilot signal (PB) will be the mixed signal of f4 (left side) and f2 (right side) from the neighboring tracks in addition to f1. The two difference frequency components are extracted by converting the PB and REF into a spectrum with mixer circuit.

f1–f4=46 kHz
f1–f2=16 kHz

The level of 46 kHz and 16 kHz are proportional to the f4 and f2 levels, respectively. The 46 kHz and 16 kHz components are extracted by the BPF at the next stage and the level is detected.
46 kHz increases when the video head is shifted in the f4 (left) direction and 16 kHz increases when shifted in the f2 (right) direction.
An amount of shift can be detected by comparing the level difference of 46 kHz and 16 kHz.
When REF is f1 and the trace position of the head shifts from the A position (origin) in the following sequence;

A=>B (+p)=>C (+–2p)=>D (+3p=–p),

the level of 46 kHz and 16 kHz components change as shown in Fig. 7-15.
When REF is changed, the reference point will change. When REF is f2, the B position is the origin for obtaining the detection characters, C for f3, and D for f4. (Table 7-3.)
Thus, REF cycles between;

f1=>f2=>f3=>f4=>,

for each track (field), and the detection reference point (origin) moves to;

A=>B=>C=>D=>,

at the switching point.

Mistracking / Reference (REF)	–2p	–p	0	+p	+2p
f1	C	D	A	B	C
f2	D	A	B	C	D
f3	A	B	C	D	A
f4	B	C	D	A	B

Table 7-3.

As shown in Fig. 7-15, the relation between levels (16 kHz/46 kHz) and directions (right and left) is reverse depending on the REF position; in case of f1 or f3 position, or in case of f2 or f4 position.

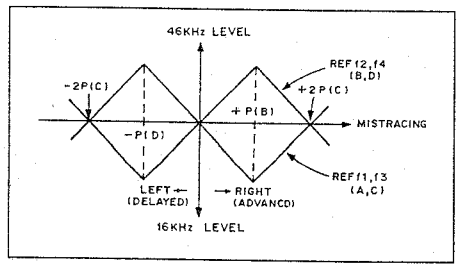


Fig. 7-15.

When the tape speed decreases and the head shifts to the left, the 46 kHz level increases at the A and C positions and the 16 kHz at the B and D positions. To the contrary, when the tape speed increases and the head shifts to the right, the 46 kHz level increases at the A and C positions or the 16 kHz at the B and D positions.
Fig. 7-16. shows above processing.

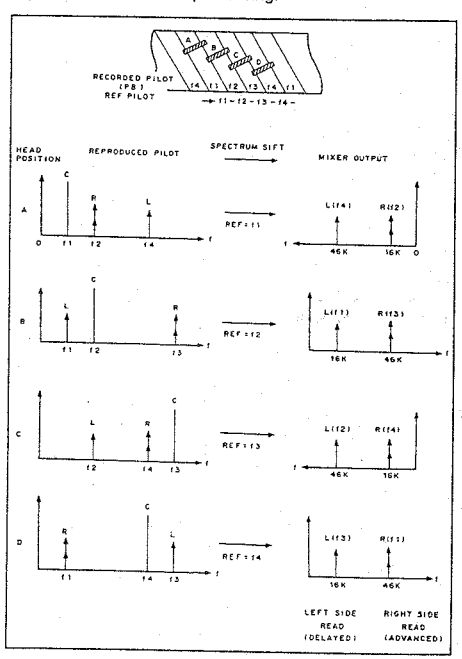


Fig. 7-16.

By means of the inverted SW control signal (16k/46k), 46 kHz and 16 kHz are compared at +/– polarity when REF is f1 or f3 position and at –/+ polarity when REF is f2 or f4 position. Thus, the compared signal has the character that the output voltage corresponds to the tape speeds.
The signal detected in this manner is called the ATF error signal.
When controlling the power supplied to the capstan motor according to the ATF error voltage, tracking centered on the origin is possible.
This is the principle of tracking with ATF function.

7-6-2. Actual Circuit Operation

ATF processing is performed by LV4050W (IC361).
The schematic diagram is shown in Fig. 7-17.

LV4050W (IC361) is divided into the recording pilot signal generation block, the playback reference pilot signal generation block and the error detection block.

[Recording]
Four pilot signals are generated by dividing the 11.7 MHz crystal oscillator output. The division ratio is selected by the two select signals (SEL1: Pin ⑦ input, SEL2:Pin ⑨ input). The relationship between SEL1 and SEL2 and the pilot signals is shown in Table 7-2. SEL1 and SEL2 signals are output from Pins ⑱ and ⑰ of CXP80720.
The recording pilot signal output from Pin ⑥ of IC361 is waveform-shaped to a sine wave by the LPF composed of ope-amp in which the IC is built in and both YC (Video) and AFM (Audio) signals are recorded on the tape.
[Playback]
The YC and the AFM components (Fc=200 kHz) of the signal output from the playback amplifier is removed by the LPF composed of inductor (L3601) and capacitor (C3618), it is input to Pin ㊽ of LV4050W (IC361). It passes through the mixer, BPF and comparator, etc., and is finally output as ATF error signal from Pin ㉑.
The ATF error signal is fed to the Analog input Pin ㉜ of CXP80720 (IC351). Input signal is AD converted, processed with the capstan motor speed detection data, converted into the PWM signal as servo data, and is output. (CAP. PWM: Pin ㉕)
Similar to the servo control operation in the recording mode, optimum tracking is performed.

7-6-3. ATF Lock Signal and Automatic Tape Speed Setting

In addition to SP (Standard-Play) mode, LP (Long-Play) mode which records by the 1/2 tape speed can be also applied in this apparatus.
Tape speed is automatically set up in order to play back by the same mode as recording.
To distinguish the kinds of recording tapes (SP/LP), use the ATF error signal. When the tape runs with the same speed as recording, and the tracking performs properly, ATF error signal is hold at a certain level.
But when the tape runs with different speed as recording, the ATF error signal's level moves up and down with a certain cycle.
This movement is detected by the main controller, and the optimum tape speed is set up properly. ATF-LOCK signal output from Pin ㉚ on IC361 (LV4050W) is input to Pin ⑰ on th controller ICX351 (CXP80720) by the signal which has adsjusted the error signal to the optimum waveform and changed to the logical level.
The signal in optimum tracking condition (Lock) becomes Low level.

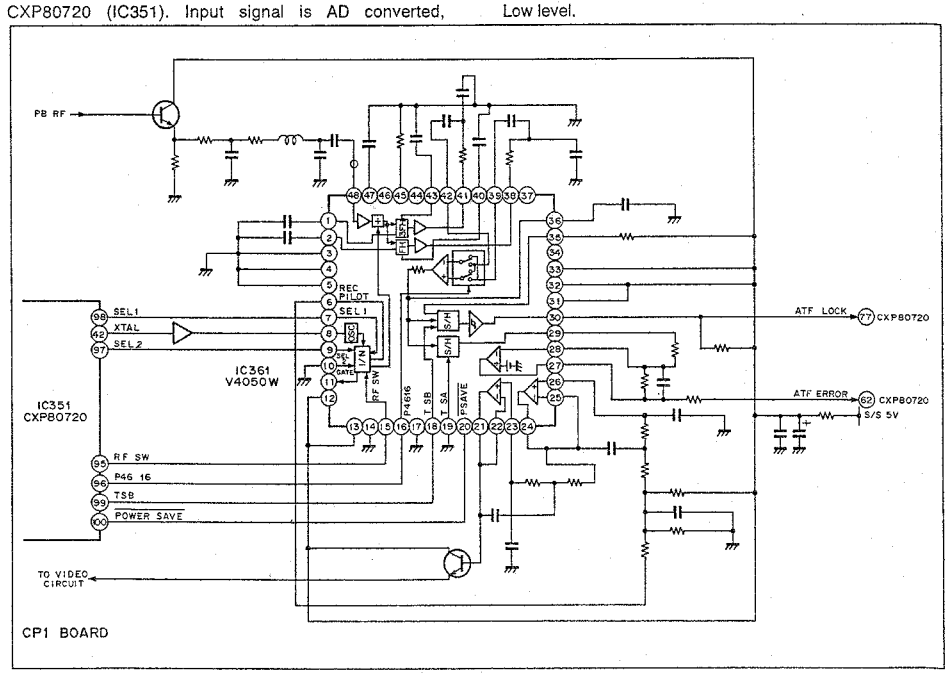


Fig. 7-17. ATF circuit

7-7. CUE/REVIEW PLAYBACK

In general, when playback a tape with "n" times speed, noise bars correspond to (n–1) tracks appear on the screen due to across (n–1) reverse azimuth tracks per one frame.
When "n" is selected to an odd number, a half the number of "n" bars will appear on the screen due to two bars overlapping at the field intervals.
When selecting the cue/review speeds to 9/–7 times the normal speed, only four noise bars will appear on the screen.

7-7-1. Tracking Phase Detection

The phase in cue/review mod is detected by ATF error signal as well as normal playback.
When the standard pilot signal Ref is changed several times in 1 field, the phase of tracking can be detected.
The servo being locked,the noise-bar is seen like standstill.

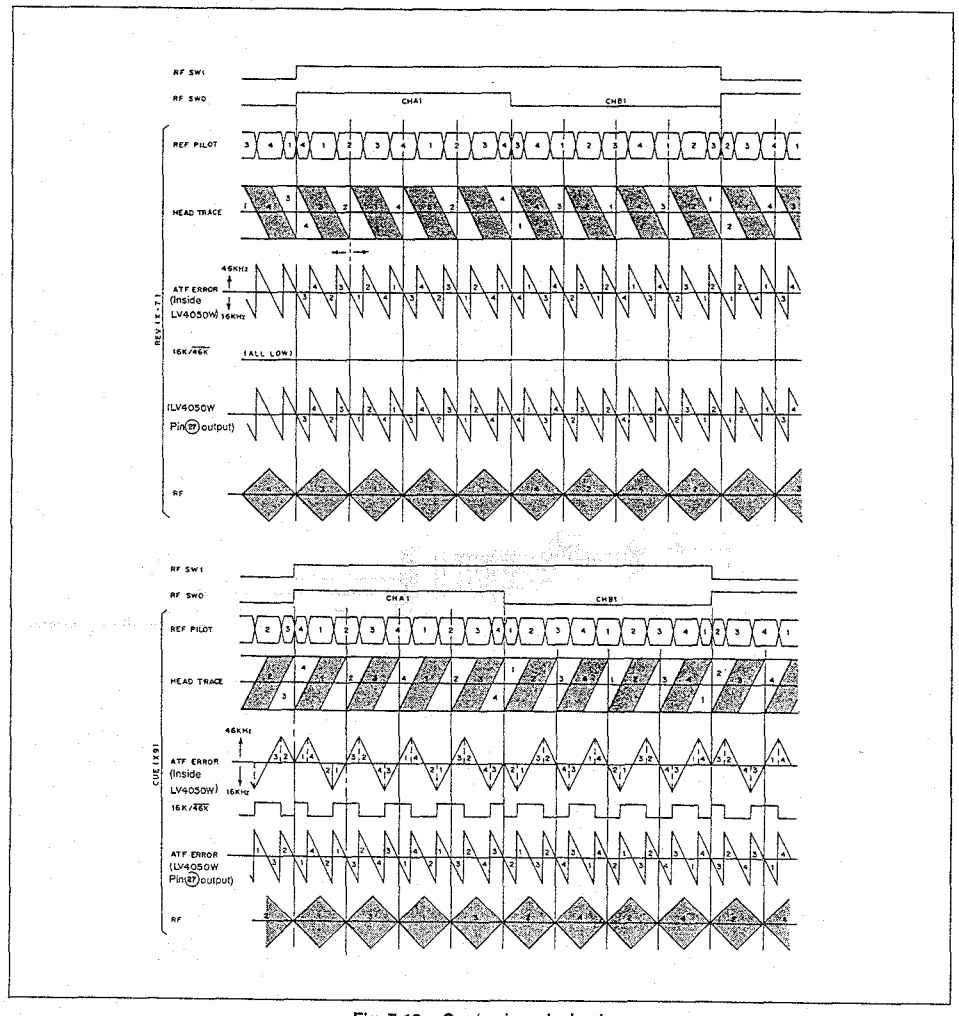


Fig. 7-18. Cue/review playback

7-7-2. Fh Correction

In cue/review playback, the relative speed between tape and heads changes and the time base of the playback video signal expands/shrinks due to the head tracing across the several tracks, causing changes in the colors, etc. In order to prevent this, the rotational speed of the drum is slightly altered to correct to the same relative speed as normal playback.
An fh correction refers to making the playback horizontal sync frequencies the same.
The rotational speed correction factor is given by the following equation:

$r = 625/(625 - 2\,\alpha H * (n-1))$ $\quad \alpha H = 2$ (SP), $= 1$ (LP)

When n=9/–7 in the cue/review, correction of approximately ± 5.3% is performed.
The tape speed (capstan rotational speed) is approximately 9/7 times after correction.
The CFG frequency is shown in Table 7-4.

System / Mode	NTSC				PAL (SP)				PAL (LP)		
	Speed	CFG (Hz)	CFG/N (Hz)	Correction	Speed	CFG (Hz)	CFG/N (Hz)	Correction	CFG	CFG/N	Correction
REC PLAY	×1	993	993	0%	×1	1389	1389	0%	694	694	0%
CUE	×9	9225	1025	3%	×9	13176	1464	5%	6588	732	+3%
REV	×–7	6748	964	–3%	×–7	9247	1321	–5%	4627	661	–3%
FRCUE	×13	13533	1041	5%	×9	13176	1464	5%	6588	732	3%
FRREV	×–11	10450	950	–4%	×–7	9247	1321	–5%	4627	661	–3%

Table 7-4. CFG Frequency

7-7-3. Pseudo Vertical Sync Signal

When the rotational speed is altered by fh correction, the frequency of the playback vertical sync signal changes. If noise appears in the vicinity of the vertical sync, vertical sync separation is lost and the vertical vibration could be cause on the screen. In order to prevent this, a pseudo vertical sync signal (JOG VD) is inserted into the video signal with the timing of the RFSW signal, during cue/review playback. JOG VD signal is output from Pin ㊾ of CXP80720 (IC351)
Fig. 7-8 shows the timing chart.